

SGM41542S Demo Board Test Report

High Input Voltage, 5A Single-Cell Battery Charger
with NVDC Power Path Management

Demo Board Pictures:

Top

Bottom

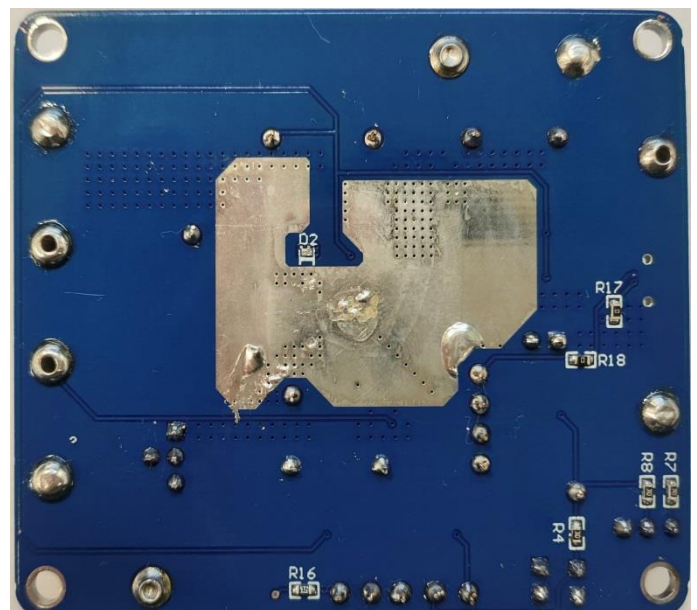
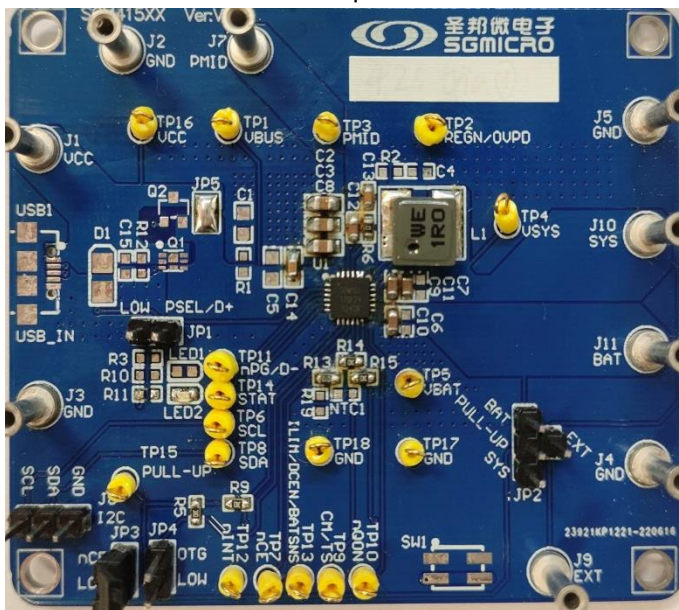


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1. Demo Board User's Guide

1.1 Test Setup for Charge Mode

1.1.1 Equipment and Jumper Cap Connection

- A. J1&J3: connecting VCC/GND to input power supply.
- B. J11&J4: connecting BAT/GND to DC power source and E-Load as emulated battery.
- C. J10&J5: connecting SYS/GND to another E-Load as emulated system load.
- D. JP3: connecting nCE to LOW.
- E. J8: connecting SCL/SDA/GND to USB dongle.

1.1.2 Register Setup

A. After hardware setup done as shown in 1.1.1, connect the USB dongle to PC, then open the SGM USB GUI interface as Fig-1, choose the “SGM41516S_42S” and click “Entry” button to enter the GUI interface.

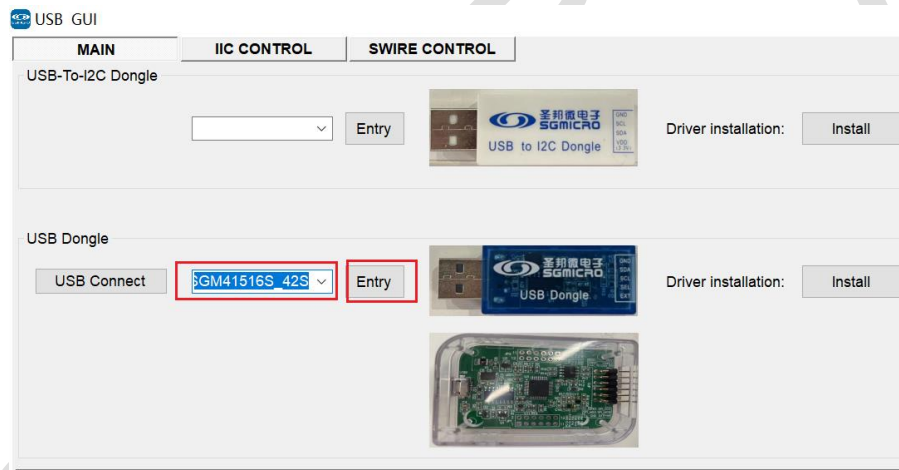


Fig-1: SGM USB GUI Interface

B. After entering the SGM41542S GUI interface as shown in Fig-2, choose the COM port and click the “Open Serial” button, then the bottom left corner of the page will display “Serial port opened” firstly. Next, choose the slave address “0x6B” and click the “Read All” button, if “Device Read OK!” is displayed, it means the I2C communication is normal.

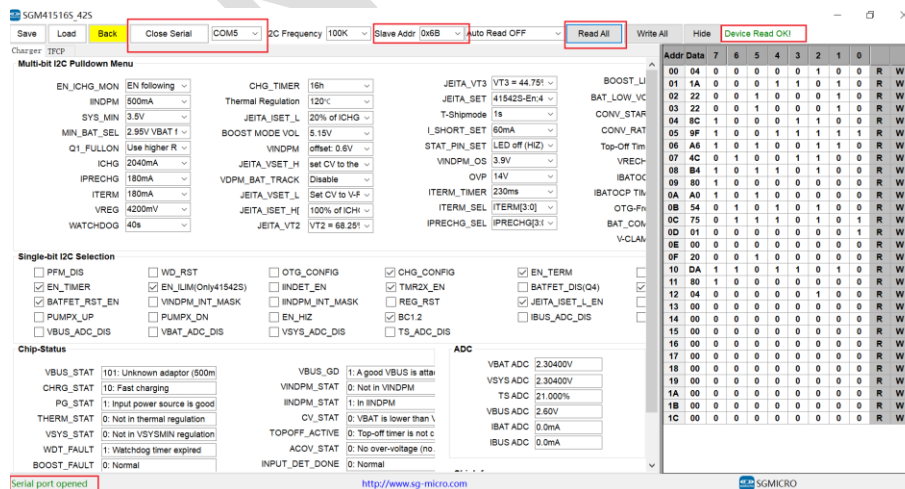


Fig-2: SGM41542S GUI Interface

1.2 Test Setup for OTG Mode

1.2.1 Equipment and Jumper Cap Connection

- A. J1&J3: connecting VCC/GND to E-Load.
- B. J11&J4: connecting BAT/GND to DC power supply.
- C. JP2: connecting PULL-UP to BAT or SYS or EXT to pull up OTG pin.
- D. J8: connecting SCL/SDA/GND to USB dongle.

1.2.2 Register Setup

As shown in 1.1.2, users can enter SGM41542S GUI interface and check the communication is normal or not. Click OTG_CONFIG as shown in Fig-3, then the device will enter OTG mode.

The screenshot displays the SGM41542S GUI interface. At the top, there are buttons for 'Save', 'Load', 'Back', and 'Close Serial'. Below these are dropdown menus for 'COM5', 'I2C Frequency' (100K), 'Slave Addr' (0x6B), and 'Auto Read OFF'. There are also buttons for 'Read All', 'Write All', and 'Show', along with a green 'Device Write OK!' indicator.

The main area is titled 'Multi-bit I2C Pulldown Menu' and contains several columns of settings:

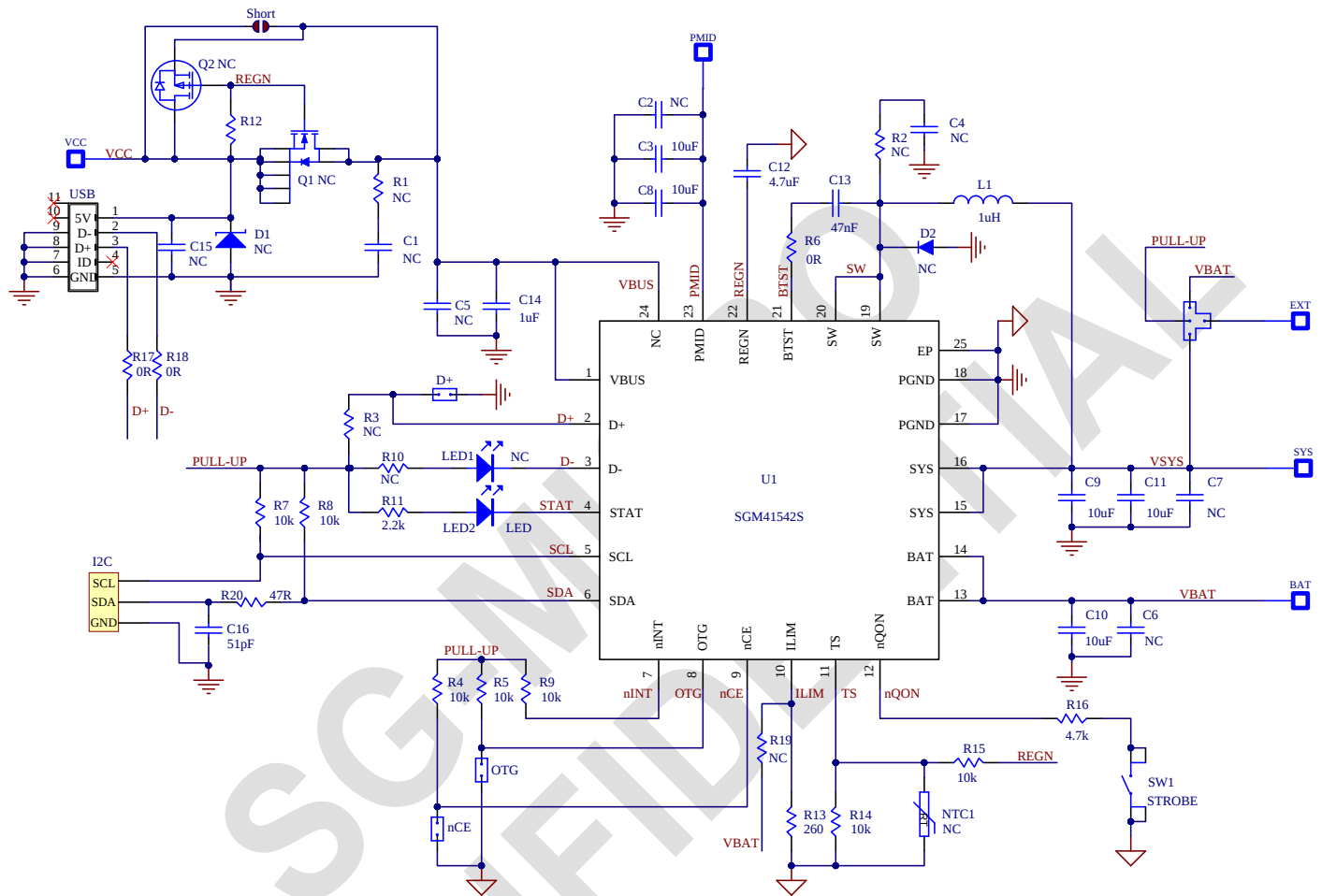
- EN_ICHG_MON**: EN following
- IINDPM**: 3300mA
- SYS_MIN**: 3.5V
- MIN_BAT_SEL**: 2.95V VBAT
- Q1_FULLON**: Use higher R
- ICHG**: 4020mA
- IPRECHG**: 180mA
- ITERM**: 180mA
- VREG**: 4200mV
- WATCHDOG**: Disable WDT
- CHG_TIMER**: 16h
- Thermal Regulation**: 120°C
- JEITA_ISET_L**: 20% of ICHG
- BOOST MODE VOL**: 5.15V
- VINDPM**: offset: 0.6V
- JEITA_VSET_H**: set CV to the
- VDPM_BAT_TRACK**: Disable
- JEITA_VSET_L**: Set CV to V-F
- JEITA_ISET_H**: 100% of ICHG
- JEITA_VT2**: VT2 = 68.291
- JEITA_VT3**: VT3 = 44.751
- JEITA_SET**: 41542S-En.4
- T-Shipmode**: 1s
- I_SHORT_SET**: 60mA
- STAT_PIN_SET**: LED off (HiZ)
- VINDPM_OS**: 3.9V
- OVP**: 14V
- ITERM_TIMER**: 230ms
- ITERM_SEL**: ITERM[3:0]
- IPRECHG_SEL**: IPRECHG[3:1]
- BOOST_LIM**: 1.2A
- BAT_LOW_VOL**: 3.15V
- CONV_START**: ADC conv not active
- CONV_RATE**: One shot
- Top-Off Timer**: Disabled
- VRECHG**: 100mV below VREG[6:0]
- IBATOCIP**: 6A
- IBATOCIP TIME**: 128us
- OTG-Freq**: 500kHz
- BAT_COMP**: 0mΩ
- V-CLAMP**: 0mV

At the bottom, there is a 'Single-bit I2C Selection' section with checkboxes for various features. The 'OTG_CONFIG' checkbox is highlighted with a red box. Other checkboxes include PFM_DIS, EN_TIMER, BATFET_RST_EN, PUMPX_UP, VBUS_ADC_DIS, WD_RST, EN_ILIM(Only 41542S), VINDPM_INT_MASK, PUMPX_ON, VBAT_ADC_DIS, INDET_EN, IINDPM_INT_MASK, EN_HI_Z, VSYS_ADC_DIS, CHG_CONFIG, TMR2X_EN, REG_RST, BC1.2, TS_ADC_DIS, EN_TERM, BATFET_DIS(IQ4), JEITA_ISET_L_EN, IBUS_ADC_DIS, EN_TSD_DISF, BATFET_DLY(T-SM_DLY), EN_PUMPX, and IBAT_ADC_DIS.

Fig-3: SGM41542S GUI Interface

1.3 Schematic, BOM List and PCB Layout

1.3.1 Schematic



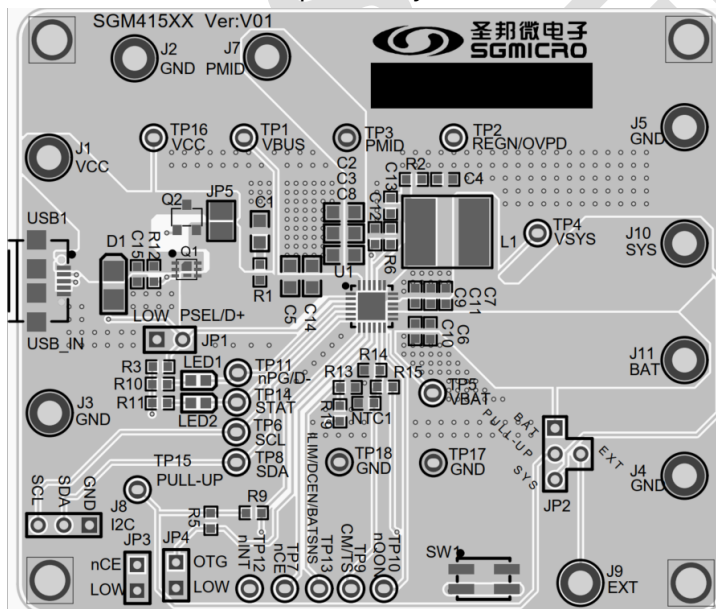
1.3.2 BOM List

Item	Designator	Quantity	Description	Manufactory
1	C1,C2,C4,C5 ,C6,C7,C15	0	NC	
2	C3,C8	2	Ceramic capacitor,10uF,25V,±10%,X5R,0805	SAMSUNG CL21A106KAYNNNE
3	C9,C10,C11	3	Ceramic capacitor,10uF,25V,±20%,X5R,0603	Murata GRM188R61E106MA73L
4	C12	1	Ceramic capacitor,4.7uF,25V,±10%,X5R,0603	Murata GRM188R61E475KE11D
5	C13	1	Ceramic capacitor,47nF,50V,±10%,X7R,0603	FH 0603B473K500NT
6	C14	1	Ceramic capacitor,1uF,25V,±10%,X5R,0603	Murata GRM188R61E105KAADD
7	C16	1	Ceramic capacitor,51pF,50V, ±5%,COG,0603	Murata

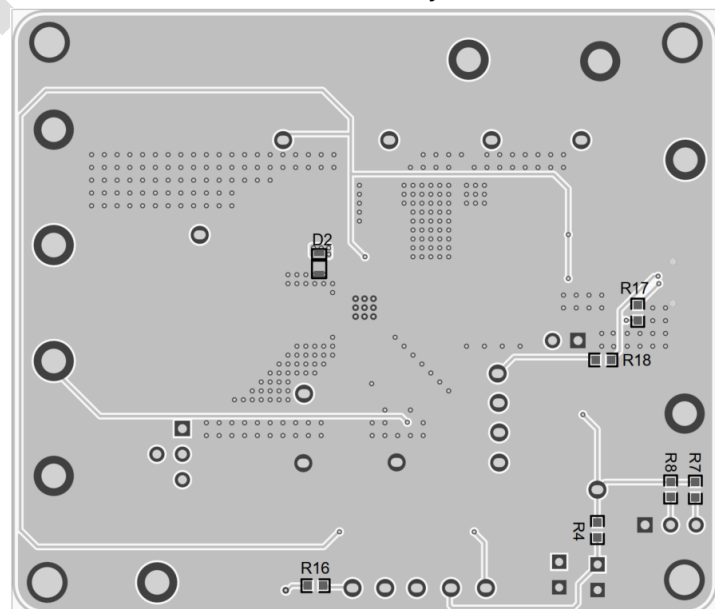
				GRM1885C1H510JA01D
8	D1,D2	0	NC	
9	L1	1	Inductor,1.0 μ H, $\pm$ 10%,I _{rms} =12A,I _{sat} =25A,DCR=5.5m Ω	WURTH 74439344010
10	LED1	0	NC	
11	LED2	1	Blue LED,0603	
12	NTC1	0	NC	
13	Q1,Q2	0	NC	
14	R1,R2,R3,R10,R12,R19	0	NC	
15	R4,R5,R7,R8,R9,R14,R15	7	Film resistor,10k Ω ,0.1W,1%,0603	
16	R11	1	Film resistor,2.2k Ω ,0.1W,1%,0603	
17	R13	1	Film resistor,260 Ω ,0.1W,1%,0603	
18	R16	1	Film resistor,4.7k Ω ,0.1W,1%,0603	
19	R6,R17,R18	3	Film resistor,0 Ω ,0.1W,1%,0603	
20	R20	1	Film resistor,47 Ω ,0.1W,1%,0603	
21	SW1	1	Tact Switch	
22	U1	1	5A Single-Cell Battery Charger with Power Path Management	SGMicro SGM41542S
Conclusion: Total 27 components.				

1.3.3 PCB Layout

Top-Side Layout



Bottom-Side Layout



2. Demo Board Test Items

2.1 Leakage Current in Ship Mode

Test conditions: $V_{BUS}=5V/9V/12V$, no battery, ship mode, HIZ mode, measure the input supply current in BUCK mode.

$V_{BUS}(V)$	$I_{BUS}(\mu A)$
5	9.882
9	18.673
12	26.856

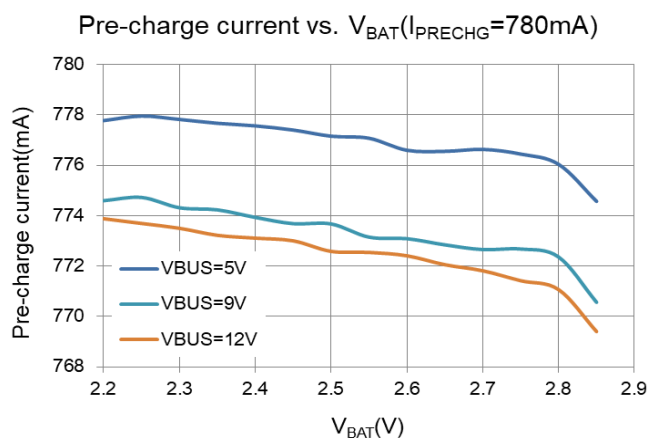
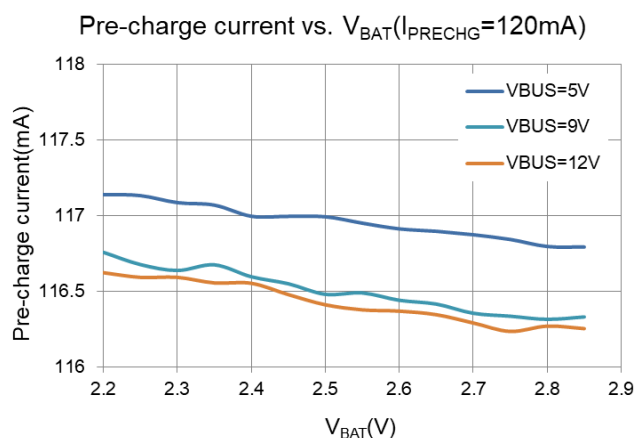
2.2 Leakage Current after Charge Termination

Test conditions: $V_{BUS}=12V$, charge termination, measure the battery current at different regulation voltage.

$V_{BAT}(V)$	$I_{BAT}(\mu A)$
4.0	16.293
4.2	16.781
4.4	17.233
4.6	17.776

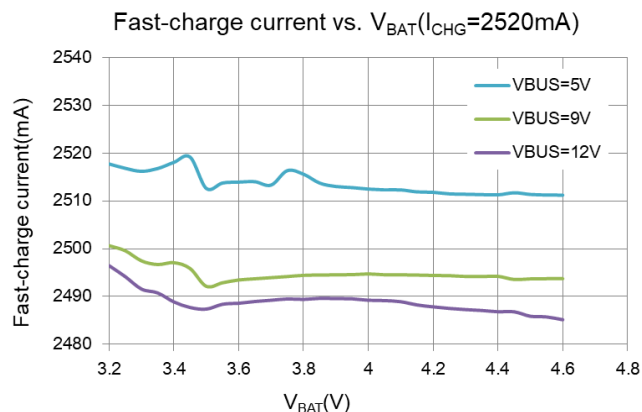
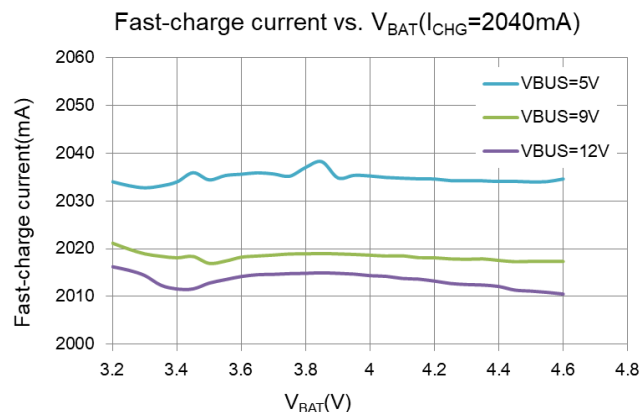
2.3 Pre-charge Current

Test conditions: $V_{BUS}=5V/9V/12V$, $V_{BAT}=2.2V\sim 2.85V$, $I_{PRECHG_SET}=120mA/780mA$, $I_{INDPM}=3.3A$, $EN_ILIM=0$, charge enable, measure the charge current at different battery voltage.



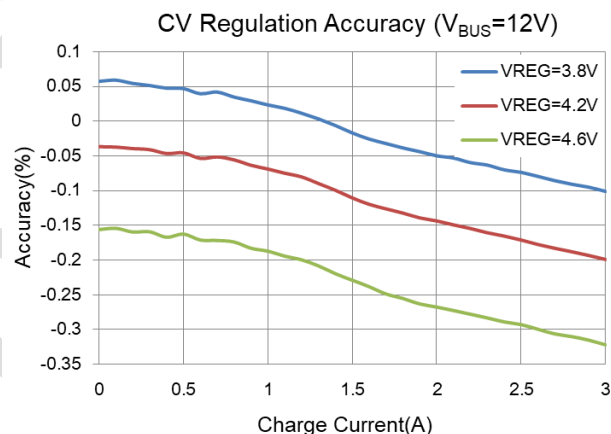
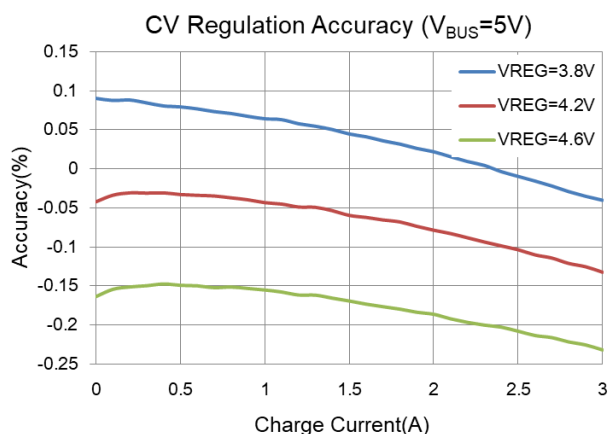
2.4 Fast Charge Current

Test conditions: $V_{BUS}=5V/9V/12V$, $V_{BAT}=3.2V\sim 4.6V$, $I_{CHG_SET}=2040mA/2520mA$, $I_{INDPM}=3.3A$, $EN_ILIM=0$, $V_{REG}=4.77V$, measure the charge current at different battery voltage.



2.5 Constant Charge Voltage Accuracy

Test conditions: $V_{BUS}=5V/9V/12V$, $V_{REG}=3.8V/4.2V/4.6V$, $I_{CHG_SET}=5040mA$, $I_{INDPM}=3.3A$, $EN_ILIM=0$, $EN_TERM=0$, charge enable, increase I_{BAT} by E-Load and measure V_{BAT} at different charge current.



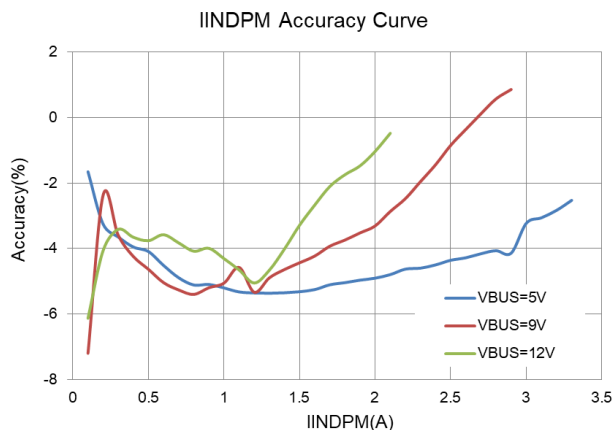
2.6 Termination Current Accuracy

Test conditions: $V_{BUS}=5V/12V$, $V_{REG}=4.2V$, $I_{CHG_SET}=2040mA$, $I_{TERM_SET}=180mA/960mA$, charge enable, adjust V_{BAT} to check termination current.

$V_{BUS}=5V$			
$I_{CHG_SET}(mA)$	$I_{TERM_SET}(mA)$	180	960
2040	$I_{TERM}(mA)$	178.131	958.161
	ACC.(%)	-1.03	-0.2
$V_{BUS}=12V$			
$I_{CHG_SET}(mA)$	$I_{TERM_SET}(mA)$	180	960
2040	$I_{TERM}(mA)$	176.344	939.3
	ACC.(%)	-2.03	-2.15

2.7 IINDPM

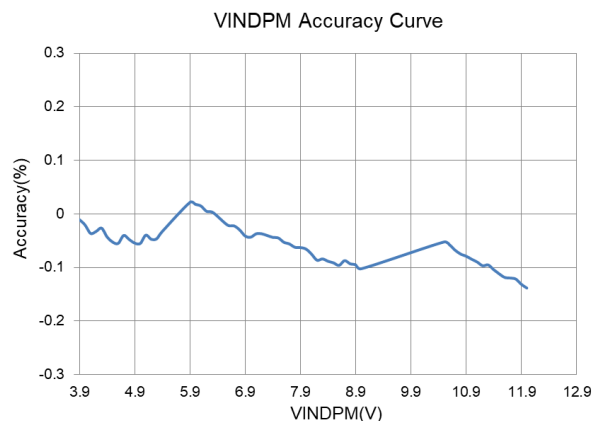
Test conditions: $V_{BUS}=5V/9V/12V$, $V_{BAT}=3.8V$, $V_{SYS_MIN}=3.5V$, charge disable, $EN_ILIM=0$, increase I_{SYS} and measure I_{BUS} to check IINDPM accuracy at different IINDPM bits setting.



Note: IINDPM accuracy of the device is trimmed as -5% of the value corresponded to register bits in the factory. The curve above illustrates the error between the measured value and the value corresponded to register bits.

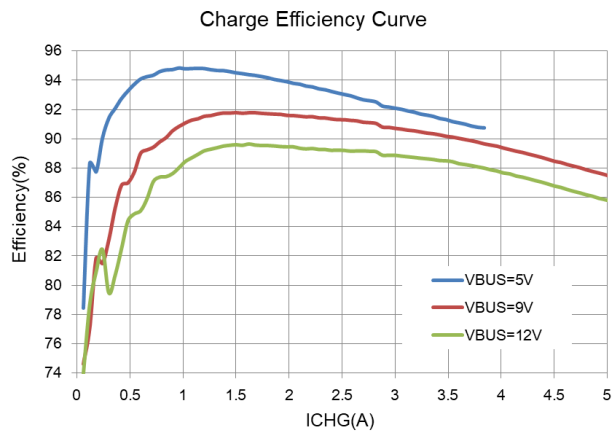
2.8 VINDPM

Test conditions: $V_{BUS}=13V/0.5A$, $V_{BAT}=3.8V$, $I_{CHG_SET}=2040mA$, $IINDPM=3.3A$, $EN_ILIM=0$, charge enable, measure V_{BUS} at different VINDPM setting.



2.9 Efficiency

Test conditions: $V_{BUS}=5V/9V/12V$, $V_{BAT}=3.8V$, $IINDPM=3.3A$, $EN_ILIM=0$, charge enable, check charge efficiency.

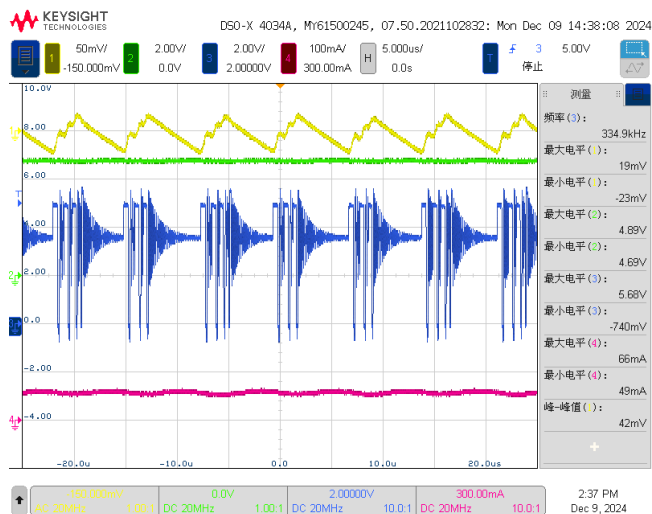
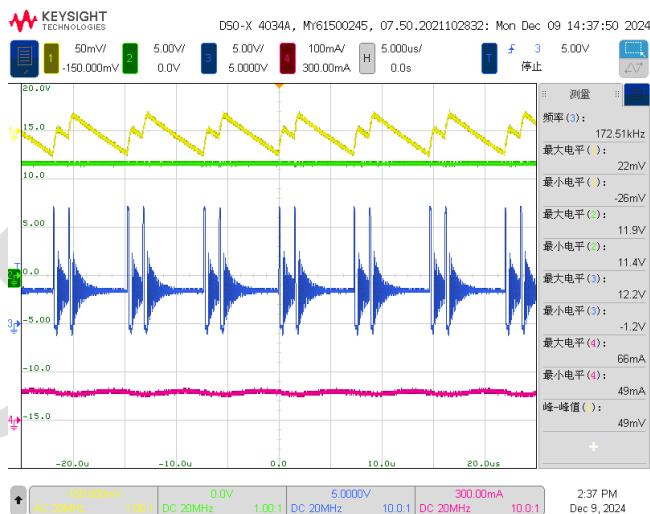


2.10 Steady State Operation

2.10.1 Charge Mode

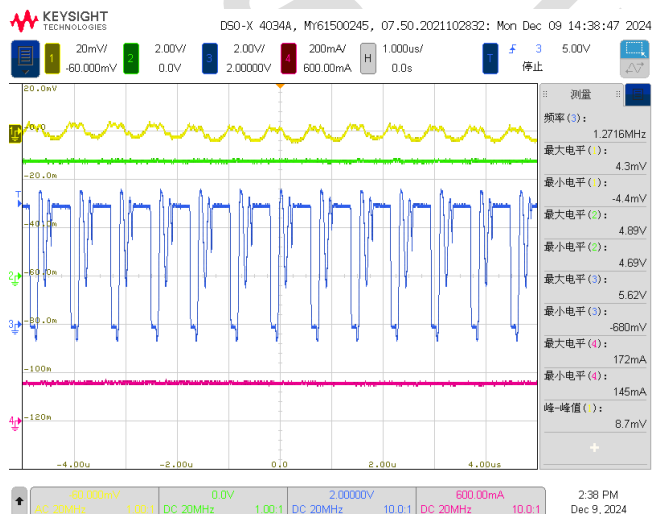
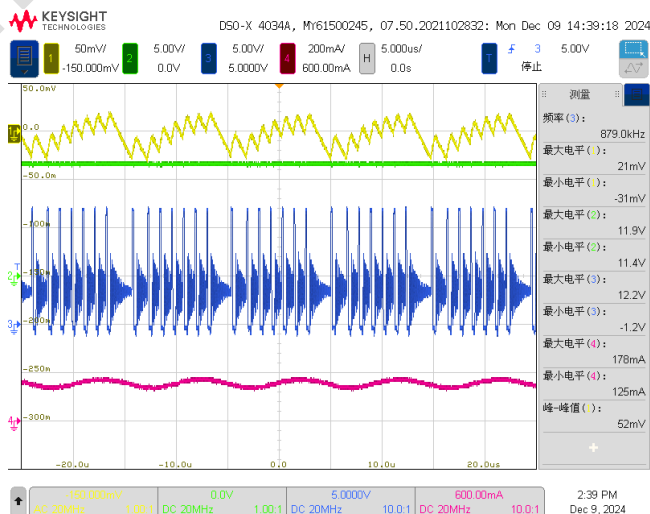
A. Trickle charge

Test conditions: $V_{BUS}=5V/12V$, $V_{BAT}=0V$, $I_{TRICHG_SET}=60mA$, charge enable.

 $V_{BUS}=5V$ CH1- $V_{SYS/ac}$, CH2- V_{BUS} , CH3- V_{SW} , CH4- I_{CHG} $V_{BUS}=12V$ CH1- $V_{SYS/ac}$, CH2- V_{BUS} , CH3- V_{SW} , CH4- I_{CHG}

B. Pre-charge

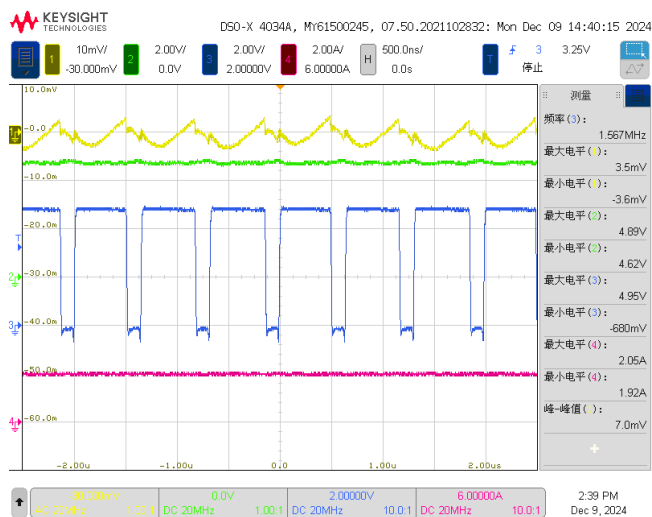
Test conditions: $V_{BUS}=5V/12V$, $V_{BAT}=2.3V$, $I_{PRECHG_SET}=180mA$, charge enable.

 $V_{BUS}=5V$ CH1- $V_{SYS/ac}$, CH2- V_{BUS} , CH3- V_{SW} , CH4- I_{CHG} $V_{BUS}=12V$ CH1- $V_{SYS/ac}$, CH2- V_{BUS} , CH3- V_{SW} , CH4- I_{CHG}

C. Fast charge

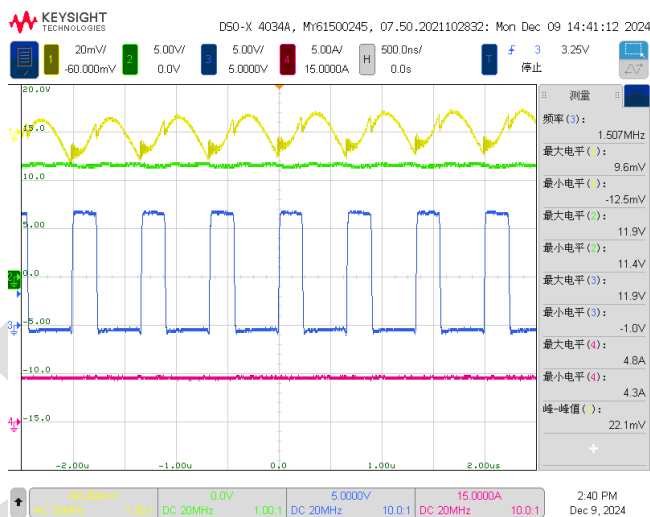
Test conditions: $V_{BUS}=5V/12V$, $V_{BAT}=3.8V$, $I_{CHG_SET}=2040/5040mA$, $I_{INDPM}=3.3A$, $EN_ILIM=0$, charge enable.

$V_{BUS}=5V$, $I_{CHG}=2040mA$



CH1- $V_{SYS/ac}$, CH2- V_{BUS} , CH3- V_{SW} , CH4- I_{CHG}

$V_{BUS}=12V$, $I_{CHG}=5040mA$

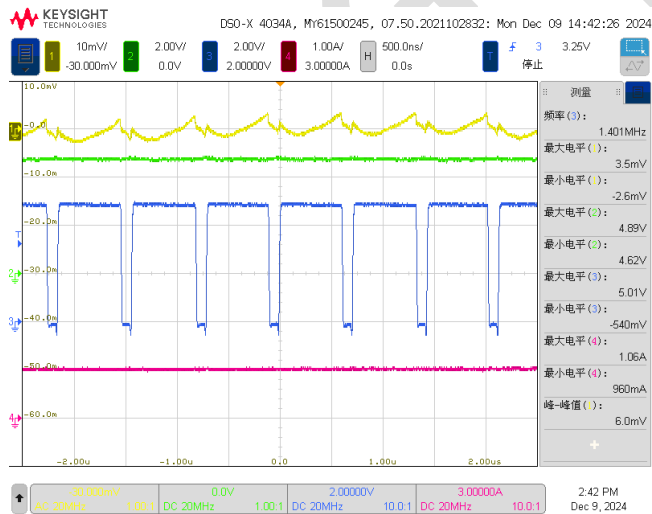


CH1- $V_{SYS/ac}$, CH2- V_{BUS} , CH3- V_{SW} , CH4- I_{CHG}

D. Constant voltage charge

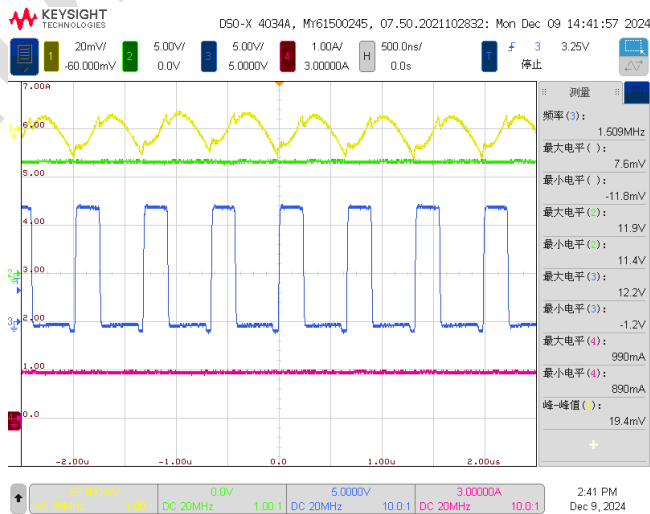
Test conditions: $V_{BUS}=5V/12V$, $V_{REG}=4.2V$, $I_{INDPM}=3.3A$, $EN_ILIM=0$, charge enable, constant voltage charge.

$V_{BUS}=5V$, $I_{CHG}=1A$



CH1- $V_{SYS/ac}$, CH2- V_{BUS} , CH3- V_{SW} , CH4- I_{CHG}

$V_{BUS}=12V$, $I_{CHG}=1A$

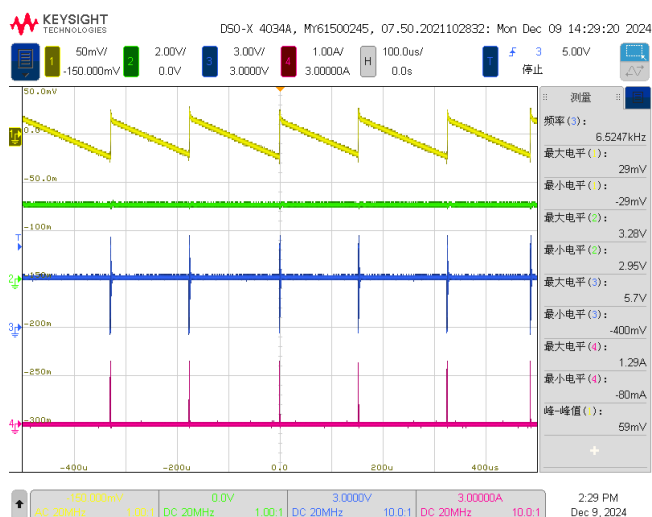


CH1- $V_{SYS/ac}$, CH2- V_{BUS} , CH3- V_{SW} , CH4- I_{CHG}

2.10.2 OTG Mode

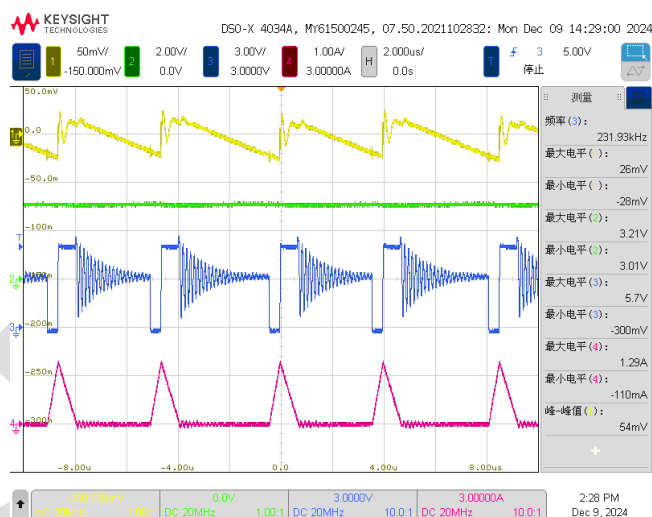
Test conditions: OTG mode, $V_{BAT}=3.3V$, $V_{BUS_SET}=5.15V$, $BOOST_LIM=3.2A$, $IBATOCPP=12A$.

$I_{BUS}=0A$



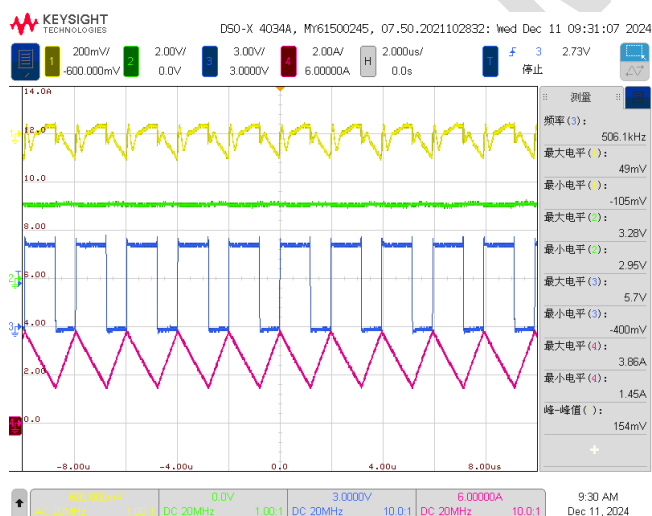
CH1- $V_{BUS/ac}$, CH2- V_{BAT} , CH3- V_{SW} , CH4- I_L

$I_{BUS}=0.1A$



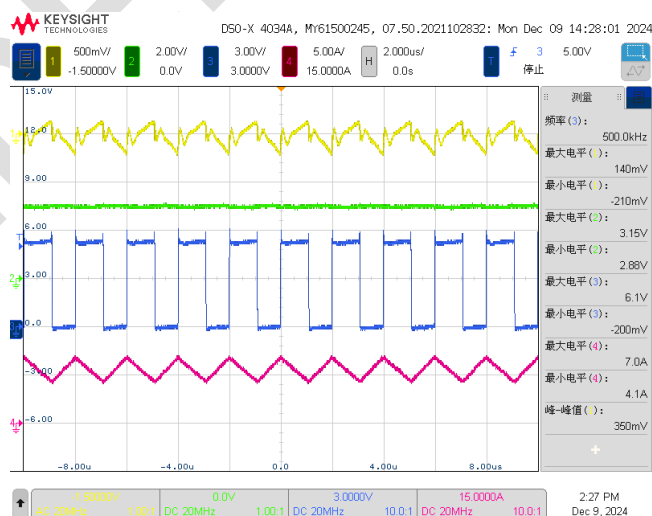
CH1- $V_{BUS/ac}$, CH2- V_{BAT} , CH3- V_{SW} , CH4- I_L

$I_{BUS}=1.6A$



CH1- $V_{BUS/ac}$, CH2- V_{BAT} , CH3- V_{SW} , CH4- I_L

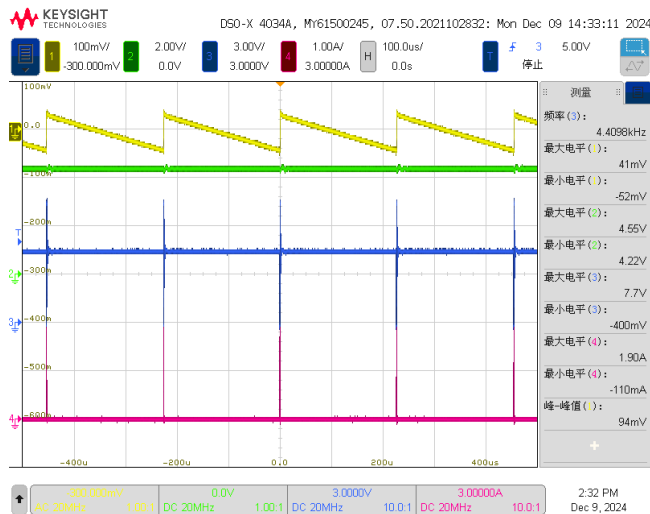
$I_{BUS}=3.2A$



CH1- $V_{BUS/ac}$, CH2- V_{BAT} , CH3- V_{SW} , CH4- I_L

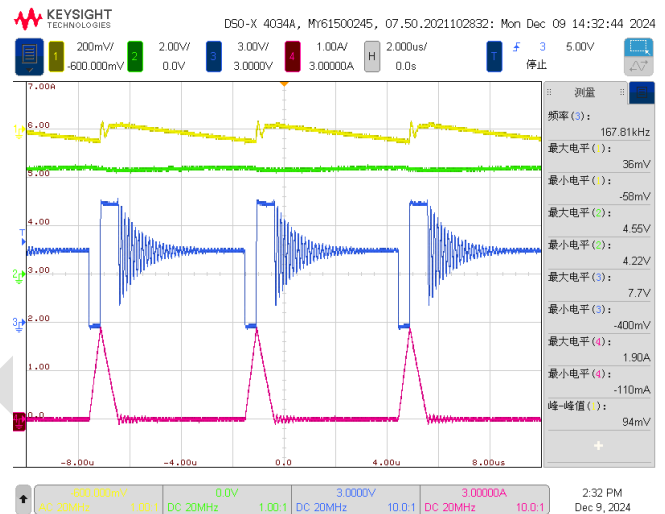
Test conditions: OTG mode, $V_{BAT}=4.6V$, $V_{BUS_SET}=7.5V$, $BOOST_LIM=3.2A$, $IBATOC=12A$.

$I_{BUS}=0A$



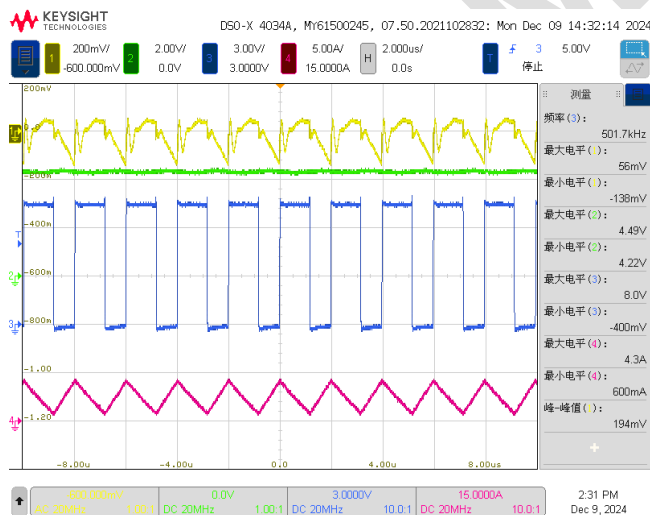
CH1- $V_{BUS/ac}$, CH2- V_{BAT} , CH3- V_{SW} , CH4- I_L

$I_{BUS}=0.1A$



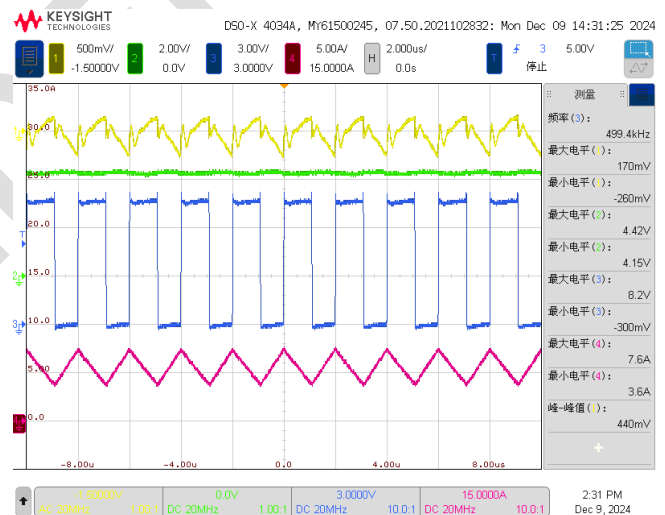
CH1- $V_{BUS/ac}$, CH2- V_{BAT} , CH3- V_{SW} , CH4- I_L

$I_{BUS}=1.6A$



CH1- $V_{BUS/ac}$, CH2- V_{BAT} , CH3- V_{SW} , CH4- I_L

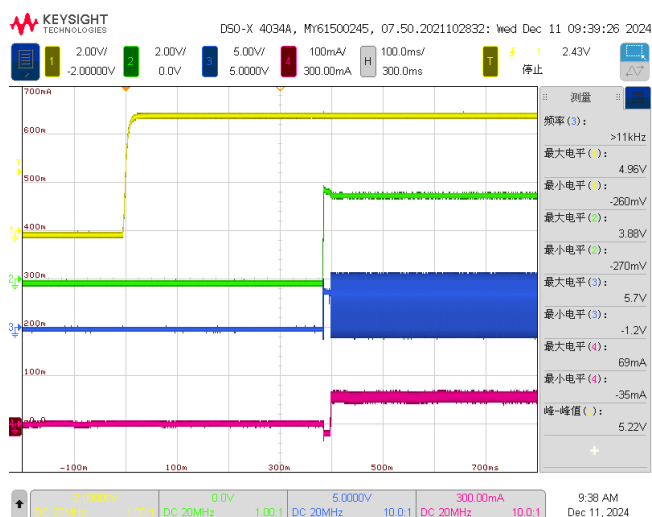
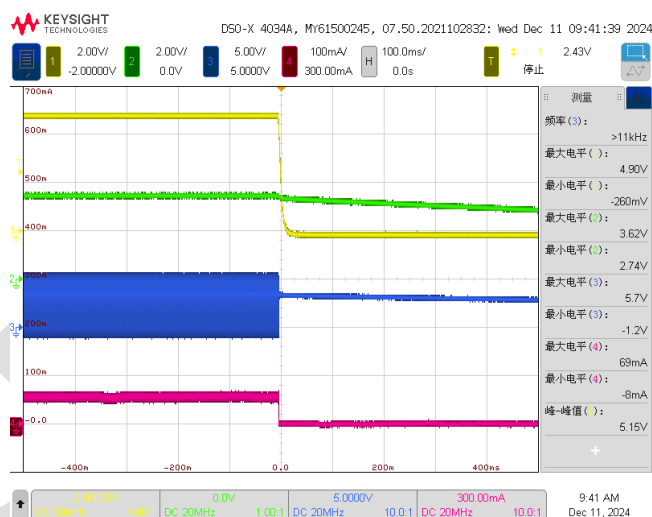
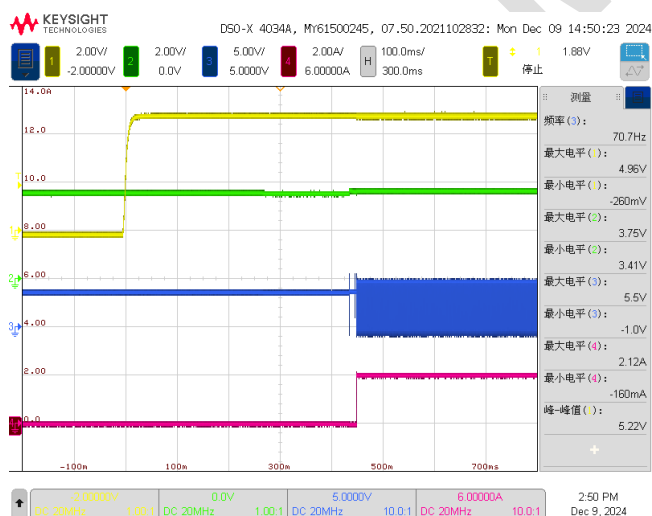
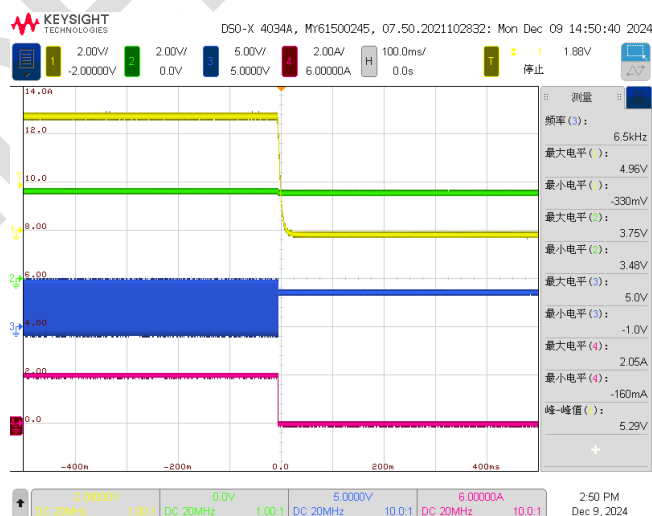
$I_{BUS}=3.2A$



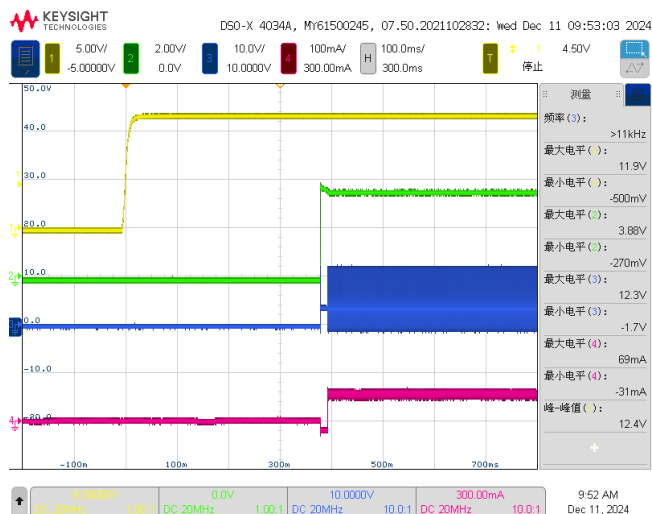
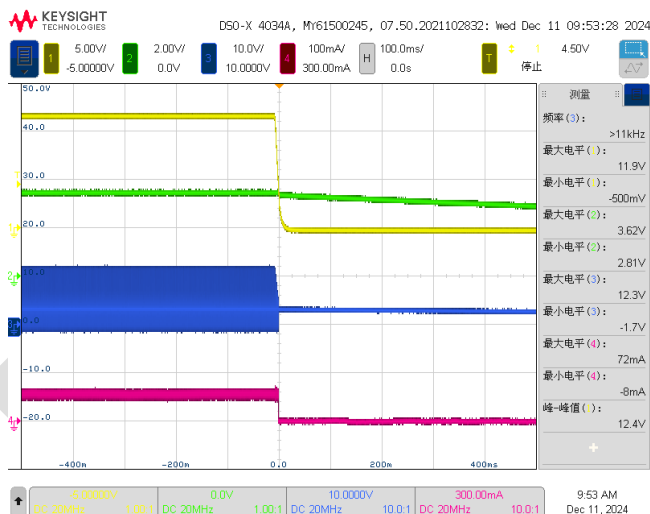
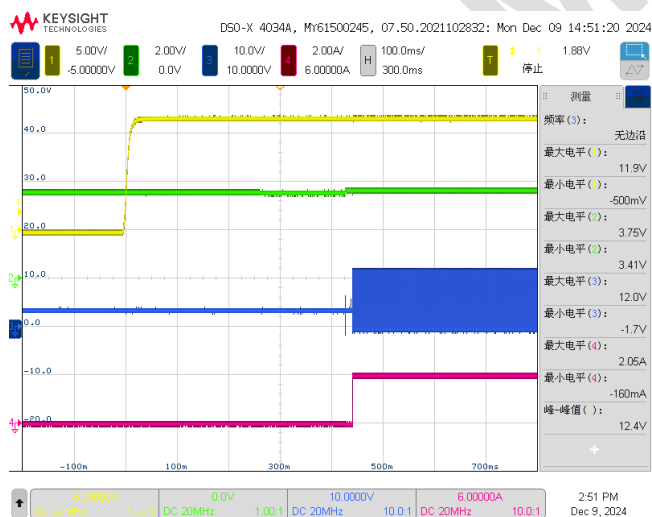
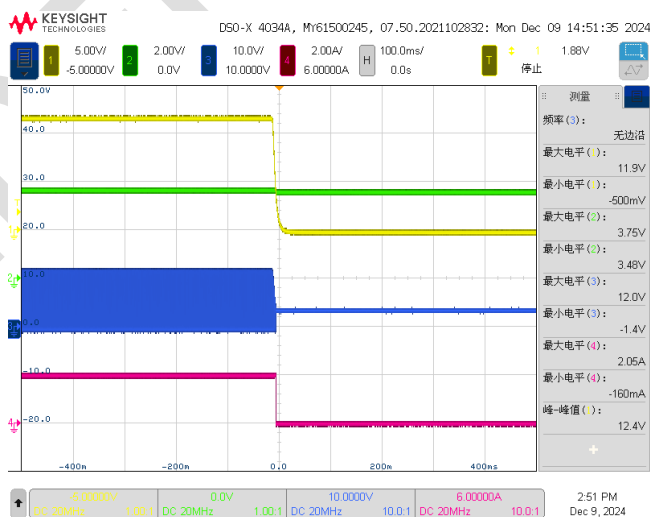
CH1- $V_{BUS/ac}$, CH2- V_{BAT} , CH3- V_{SW} , CH4- I_L

2.11 Charger Startup/Shutdown through VBUS

Test conditions: $V_{BUS}=5V$, registers default setting, DP and DM short, plug in/out adaptor at different battery voltage.

Plug in adaptor at $V_{BAT}=1.5V$ Plug out adaptor at $V_{BAT}=1.5V$ Plug in adaptor at $V_{BAT}=3.8V$ Plug out adaptor at $V_{BAT}=3.8V$ 

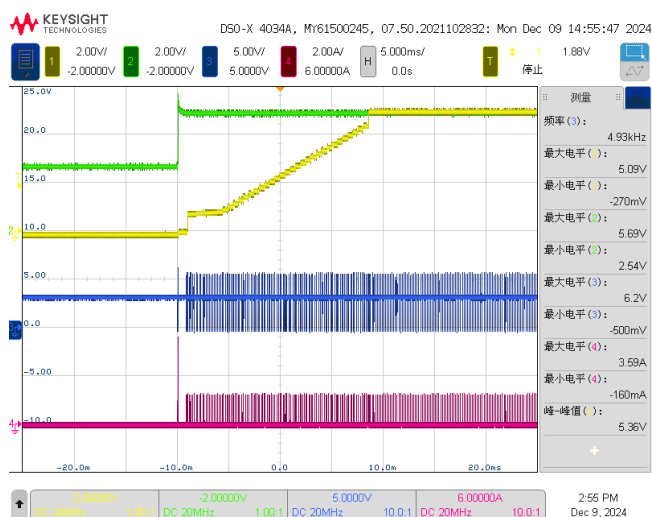
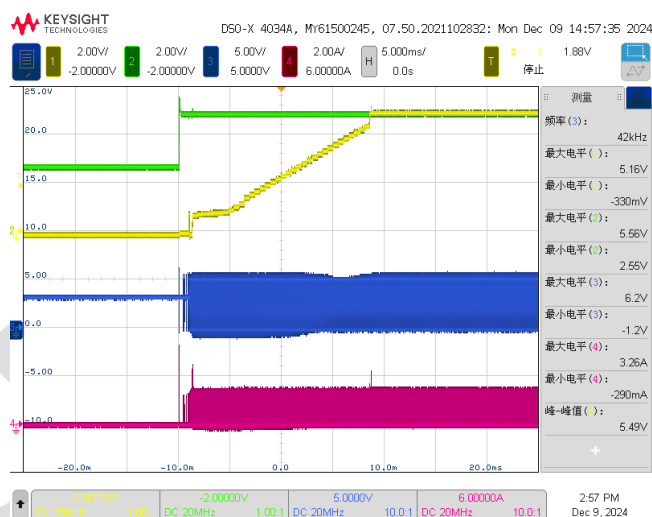
Test conditions: $V_{BUS}=12V$, registers default setting, DP and DM short, plug in/out adaptor at different battery voltage.

Plug in adaptor at $V_{BAT}=1.5V$ CH1- V_{BUS} , CH2- V_{SYS} , CH3- V_{SW} , CH4- I_{CHG} Plug out adaptor at $V_{BAT}=1.5V$ CH1- V_{BUS} , CH2- V_{SYS} , CH3- V_{SW} , CH4- I_{CHG} Plug in adaptor at $V_{BAT}=3.8V$ CH1- V_{BUS} , CH2- V_{SYS} , CH3- V_{SW} , CH4- I_{CHG} Plug out adaptor at $V_{BAT}=3.8V$ CH1- V_{BUS} , CH2- V_{SYS} , CH3- V_{SW} , CH4- I_{CHG}

2.12 Enter/Exit OTG Mode

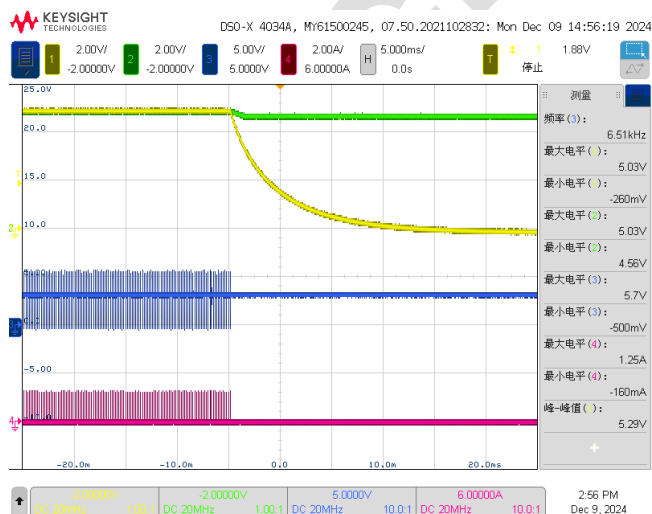
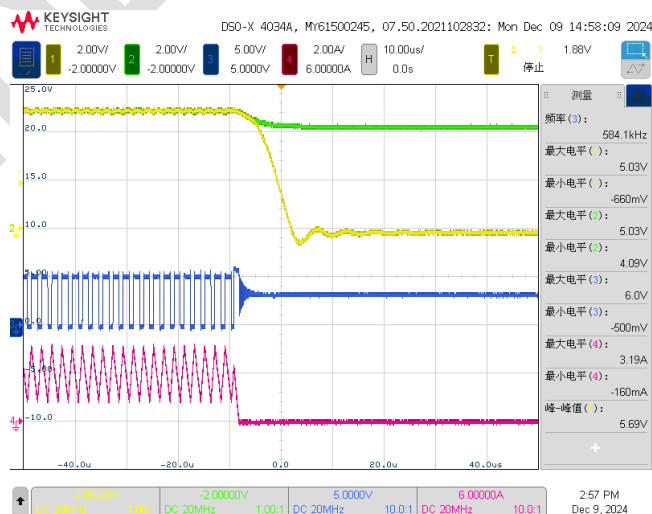
Test conditions: $V_{BAT}=3.3V$, enable OTG, enter OTG mode with different load.

Enter OTG mode, no load

CH1- V_{BUS} , CH2-PMID, CH3- V_{SW} , CH4- I_L Enter OTG mode, $I_{BUS}=0.3A$ CH1- V_{BUS} , CH2-PMID, CH3- V_{SW} , CH4- I_L

Test conditions: $V_{BAT}=3.3V$, disable OTG, exit OTG mode with different load.

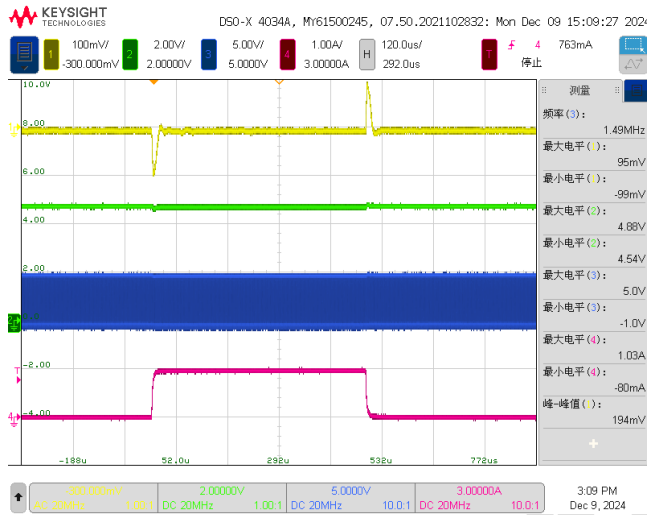
Exit OTG mode, no load

CH1- V_{BUS} , CH2-PMID, CH3- V_{SW} , CH4- I_L Exit OTG mode, $I_{BUS}=1.2A$ CH1- V_{BUS} , CH2-PMID, CH3- V_{SW} , CH4- I_L

2.13 Charger System Load Transient

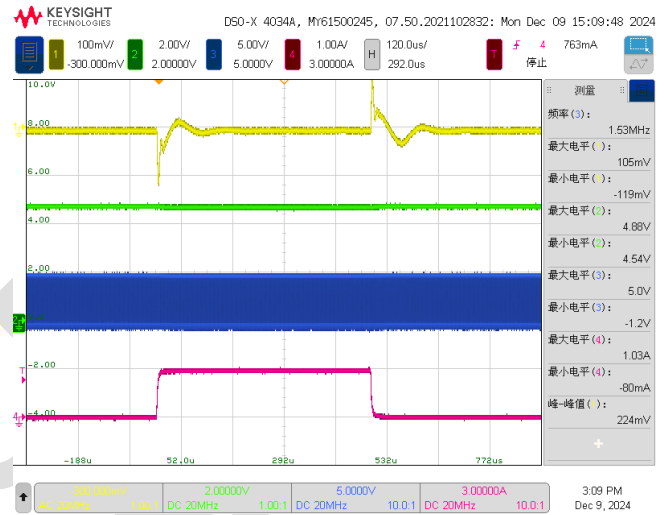
Test conditions: $V_{BUS}=5V$, $V_{BAT}=3.2V/3.8V$, $I_{CHG_SET}=2040mA$, $I_{INDPM}=3.3A$, $EN_ILIM=0$, dynamic $I_{SYS}=0A-1A-0A$ (slew rate: $1A/us$).

$V_{BAT}=3.2V$, $I_{SYS}=0A-1A-0A$



CH1- $V_{SYS/lac}$, CH2- V_{BUS} , CH3- V_{sw} , CH4- I_{sys}

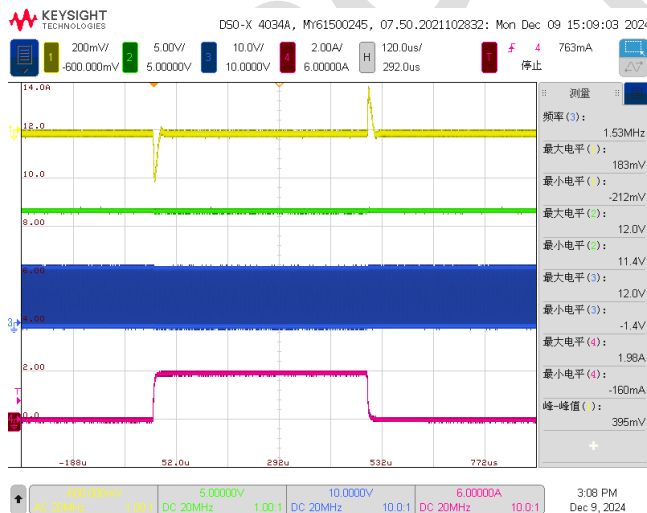
$V_{BAT}=3.8V$, $I_{SYS}=0A-1A-0A$



CH1- $V_{SYS/lac}$, CH2- V_{BUS} , CH3- V_{sw} , CH4- I_{sys}

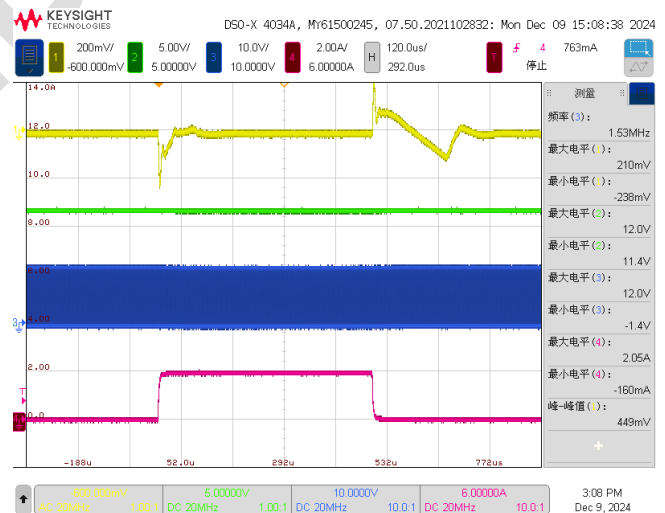
Test conditions: $V_{BUS}=12V$, $V_{BAT}=3.2V/3.8V$, $I_{CHG_SET}=2040mA$, $I_{INDPM}=3.3A$, $EN_ILIM=0$, dynamic $I_{SYS}=0A-2A-0A$ (slew rate: $1A/us$).

$V_{BAT}=3.2V$, $I_{SYS}=0A-2A-0A$



CH1- $V_{SYS/lac}$, CH2- V_{BUS} , CH3- V_{sw} , CH4- I_{sys}

$V_{BAT}=3.8V$, $I_{SYS}=0A-2A-0A$



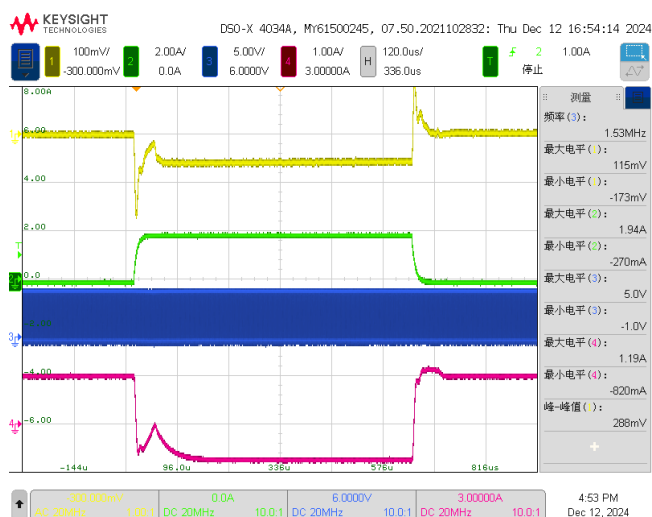
CH1- $V_{SYS/lac}$, CH2- V_{BUS} , CH3- V_{sw} , CH4- I_{sys}

SGM41542S

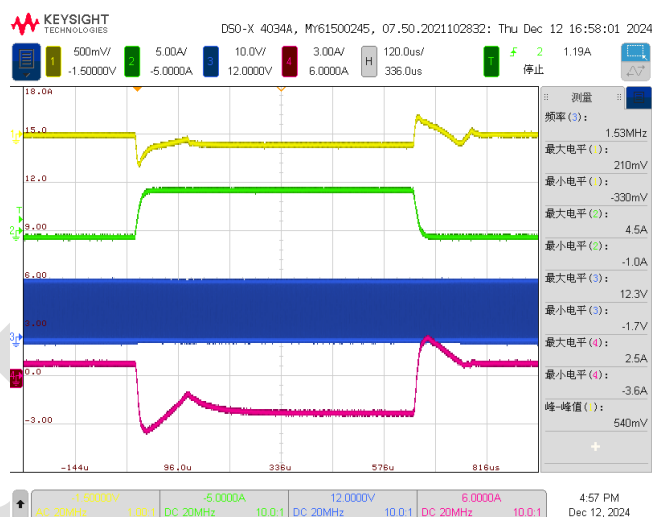
Demo Board Test Report

Test conditions: $V_{BUS}=5V/12V$, $V_{BAT}=3.8V$, $I_{CHG_SET}=1020mA$, $I_{INDPM}=1000mA$, $EN_ILIM=0$, dynamic $I_{SYS}=0A-1A-0A/0A-5A-0A$ (slew rate: $1A/us$).

$V_{BUS}=5V$, $I_{SYS}=0A-2A-0A$



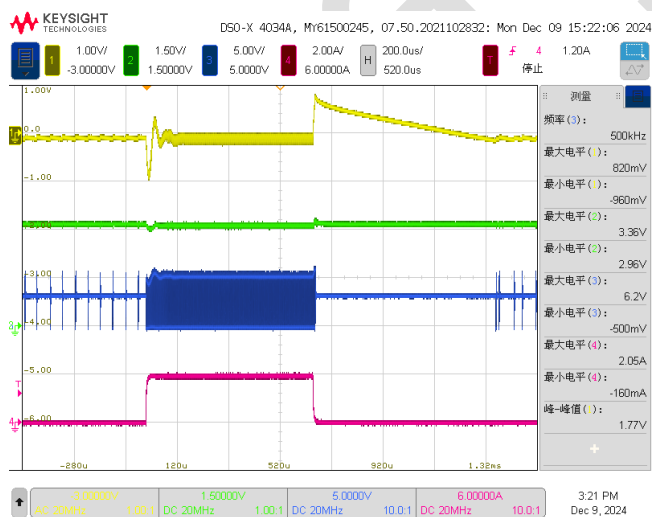
$V_{BUS}=12V$, $I_{SYS}=0A-5A-0A$



2.14 OTG Load Transient

Test conditions: OTG mode, $V_{BAT}=3.3V$, $V_{BUS}=5.15V$, $BOOST_LIM=3.2A$, $I_{BUS}=0A-2A-0A/1A-2A-1A$ (slew rate: $1A/us$).

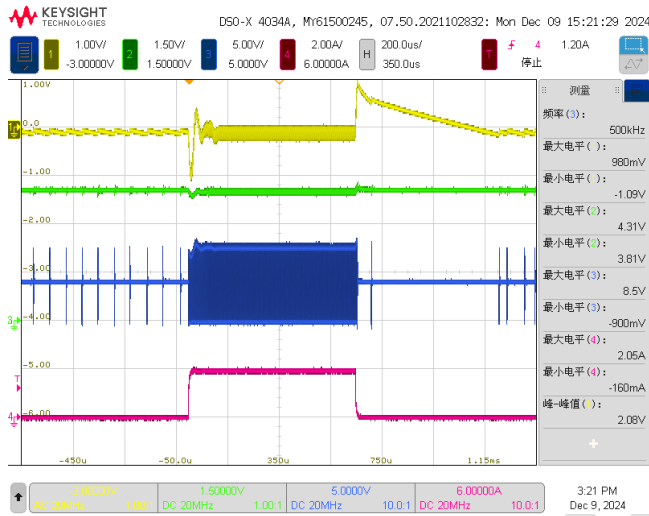
$I_{BUS}=0A-2A-0A$



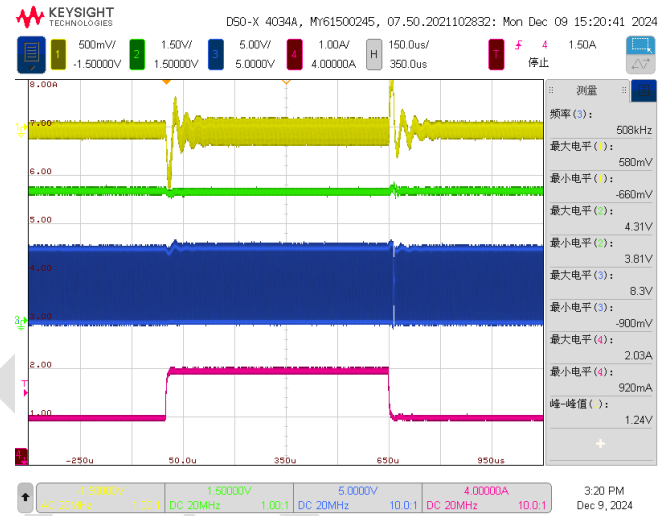
$I_{BUS}=1A-2A-1A$



Test conditions: OTG mode, $V_{BAT}=4.2V$, $V_{BUS}=7.5V$, $BOOST_LIM=3.2A$, $I_{BUS}=0A-2A-0A/1A-2A-1A$ (slew rate: 1A/us).

 $I_{BUS}=0A-2A-0A$ 

CH1- $V_{BUS/ac}$, CH2- V_{BAT} , CH3- V_{SW} , CH4- I_{BUS}

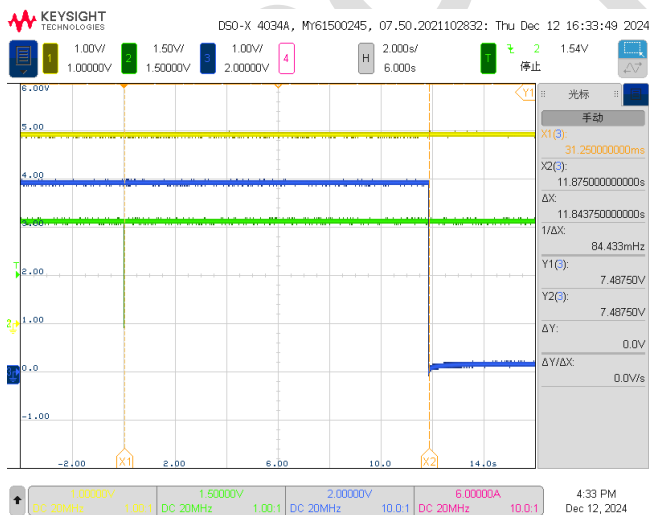
 $I_{BUS}=1A-2A-1A$ 

CH1- $V_{BUS/ac}$, CH2- V_{BAT} , CH3- V_{SW} , CH4- I_{BUS}

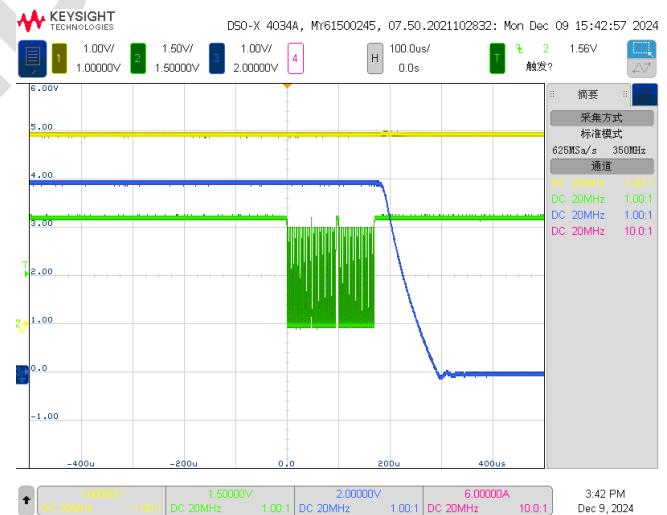
2.15 Enter/Exit Ship Mode

A. Enter ship mode

Test conditions: $V_{BAT}=4V$, VSYS connect to E-Load with 0.5A load in CC mode. Write $BATFET_DIS=1$ to enter ship mode with different delay time.

 $BATFET_DLY=1$ 

CH1- V_{BAT} , CH2-SCL, CH3- V_{SYS}

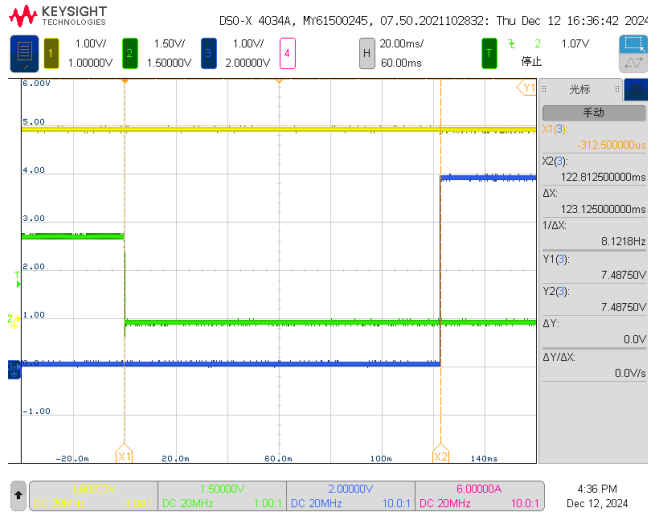
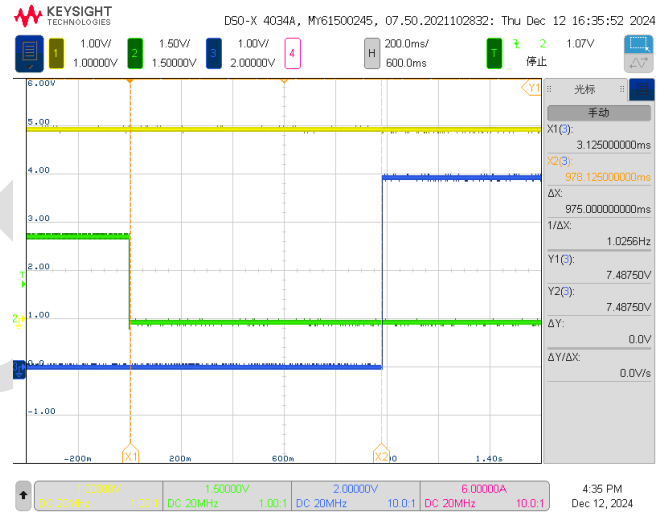
 $BATFET_DLY=0$ 

CH1- V_{BAT} , CH2-SCL, CH3- V_{SYS}

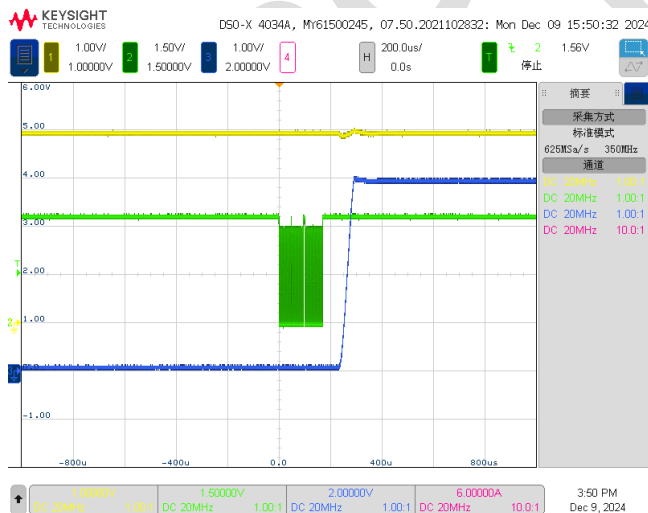
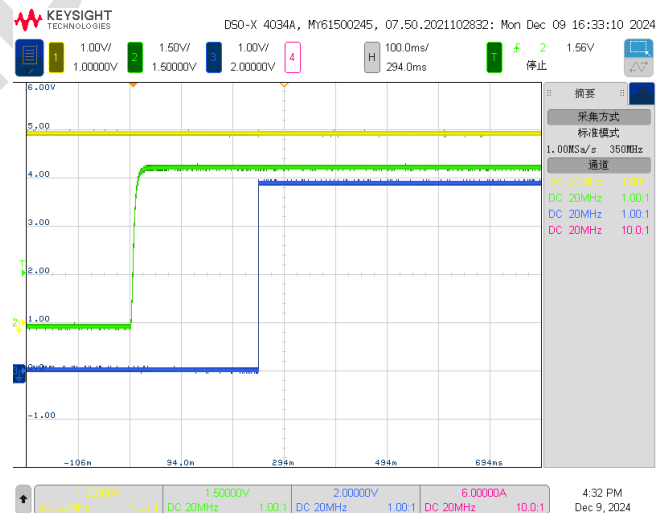
B. Exit ship mode

Test conditions: $V_{BAT}=4V$, SYS connect to E-Load with 0.5A load in CC mode. Exit ship mode by:

1. Pull nQON pin from logic high to low at least $t_{shipmode}$.
2. Clear BATFET_DIS bit using I2C.
3. Plug-in V_{BUS} .

Shorting nQON to GND, $t_{shipmode}=100ms$ Shorting nQON to GND, $t_{shipmode}=1s$ 

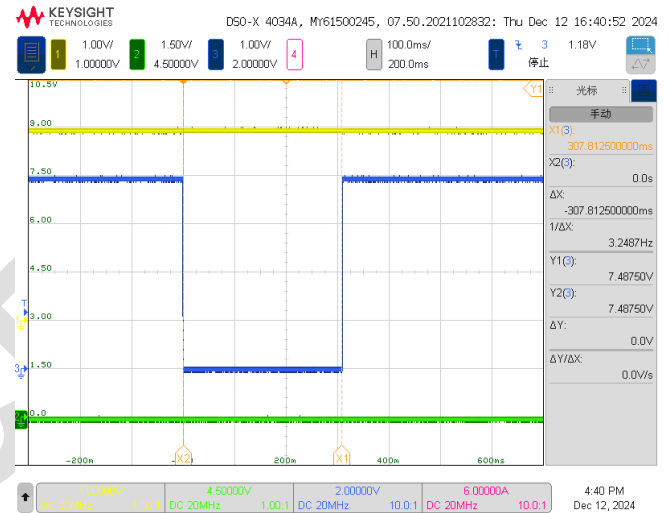
BATFET_DIS=0

Plug-in V_{BUS} 

2.16 Reset VSYS

Test conditions: $V_{BAT}=4V$, SYS connect to E-Load with 0.5A load in CC mode. Pull nQON pin from logic high to low at least 10s.

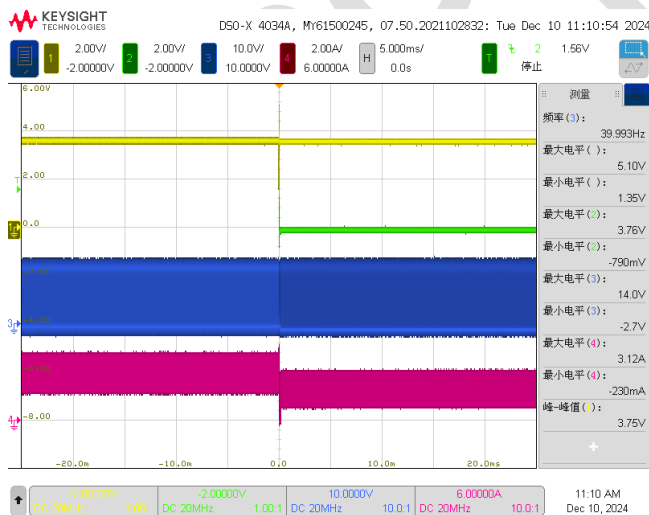
Zoom in nQON Pull Down

Zoom in V_{sys} Reset

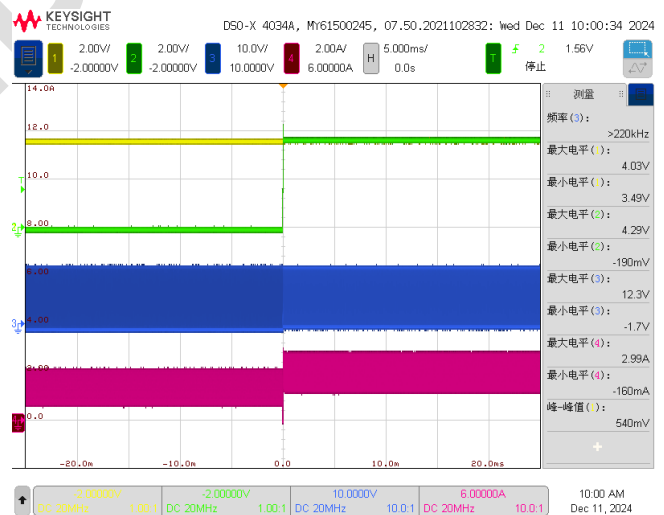
2.17 System SCP

Test conditions: $V_{BUS}=12V$, $V_{BAT}=3.8V$, $I_{CHG_SET}=2040mA$, charge enable, short system to GND, then release.

Short



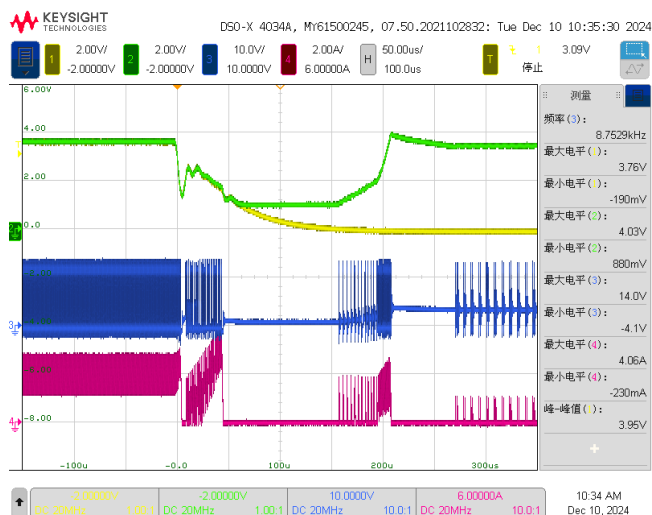
Release



2.18 Battery SCP

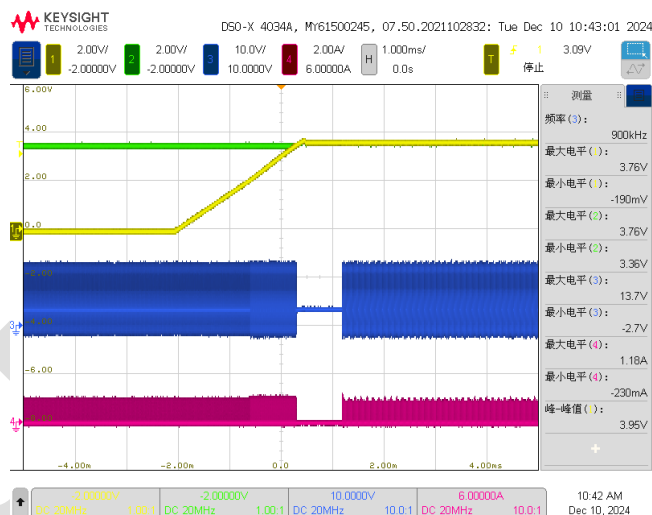
Test conditions: $V_{BUS}=12V$, $V_{BAT}=3.8V$, $I_{CHG_SET}=2040mA$, charge enable, short battery to GND, then release.

Short



CH1- V_{BAT} , CH2- V_{SYS} , CH3- V_{SW} , CH4- I_L

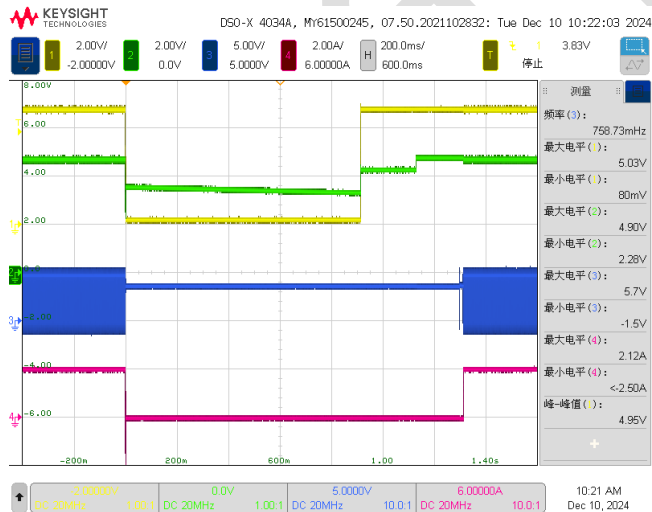
Release



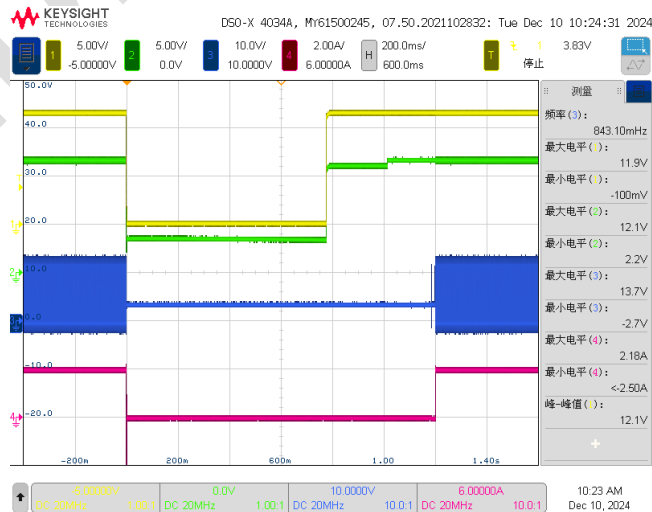
CH1- V_{BAT} , CH2- V_{SYS} , CH3- V_{SW} , CH4- I_L

2.19 VBUS SCP

Test conditions: $V_{BUS}=5V/12V$, $V_{BAT}=3.8V$, $I_{CHG_SET}=2040mA$, charge enable, short V_{BUS} to GND, then release.

 $V_{BUS}=5V$ 

CH1- V_{BUS} , CH2- P_{MID} , CH3- V_{SW} , CH4- I_{CHG}

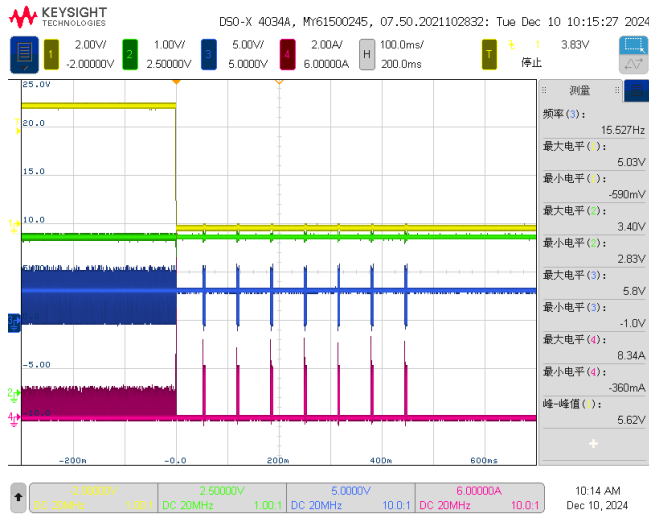
 $V_{BUS}=12V$ 

CH1- V_{BUS} , CH2- P_{MID} , CH3- V_{SW} , CH4- I_{CHG}

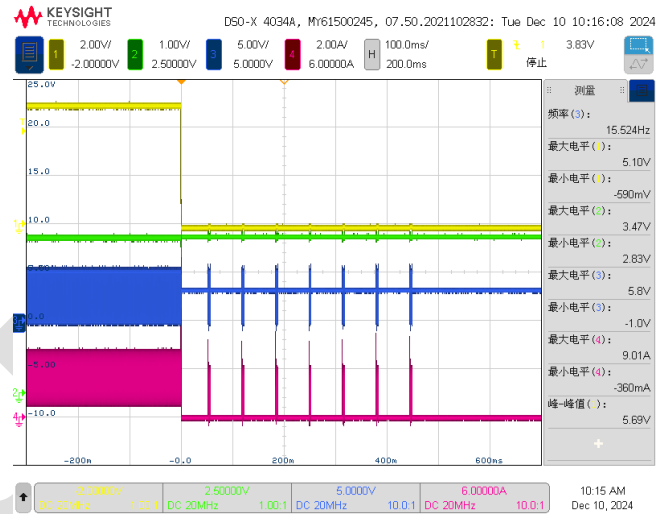
2.20 VBUS SCP&OCP in OTG Mode

Test conditions: $V_{BAT}=3.3V$, $V_{BUS_SET}=5.15V$, enable OTG mode, then short V_{BUS} to GND

$I_{BUS}=0A$, short

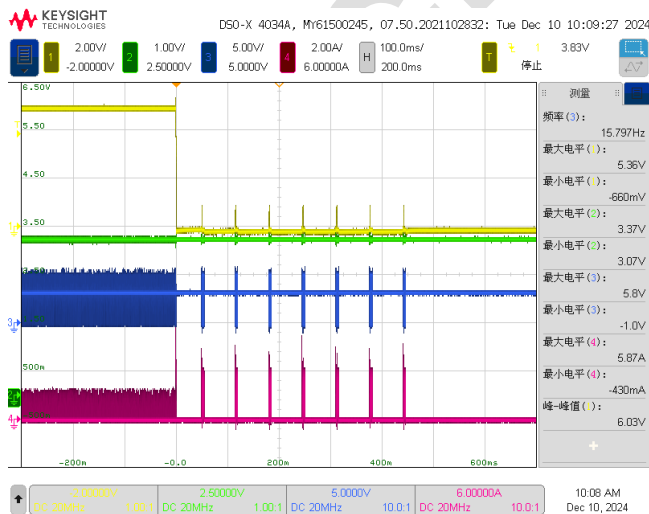


$I_{BUS}=1A$, short

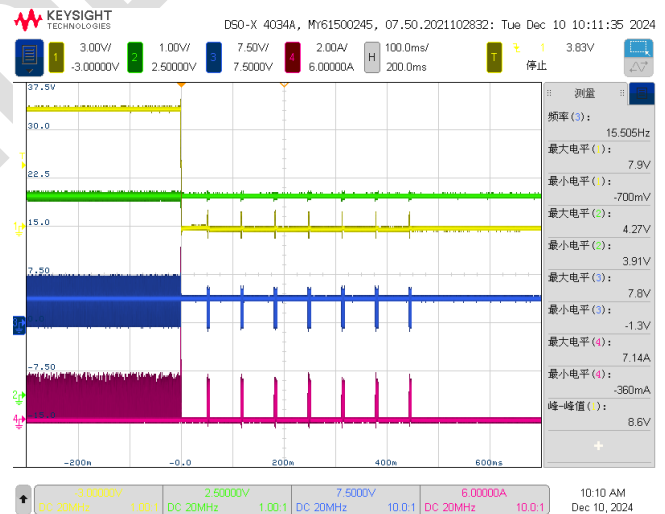


Test conditions: $V_{BAT}=3.3V/4.2V$, $V_{BUS_SET}=5.15V/7.5V$, BOOST_LIM=1.2A, enable OTG mode, increase I_{BUS} till OCP.

$V_{BAT}=3.3V$, $V_{BUS}=5.15V$



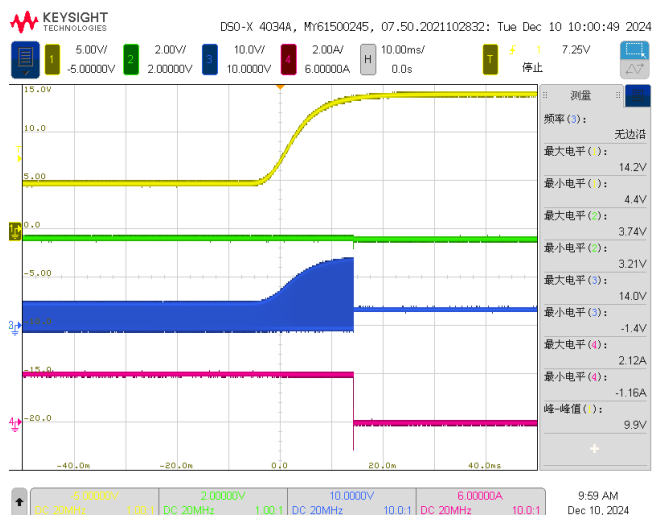
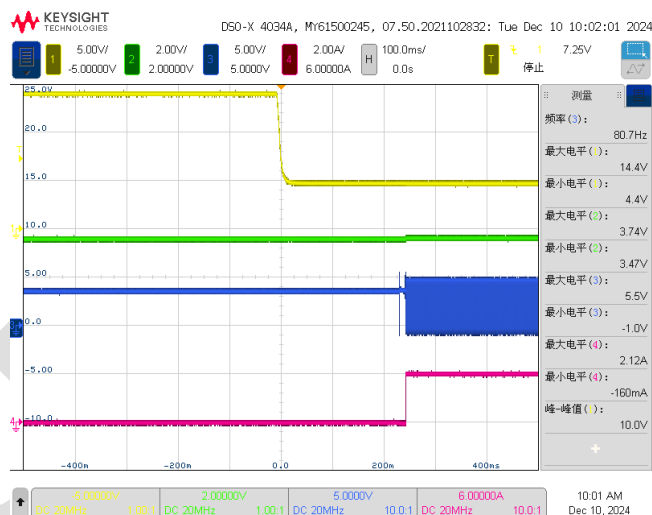
$V_{BAT}=4.2V$, $V_{BUS}=7.5V$



Note: If release the short circuit or overload before the seventh restart, OTG can restart. Release the short circuit or overload after the seventh restart, then OTG needs to be re-enabled by I2C.

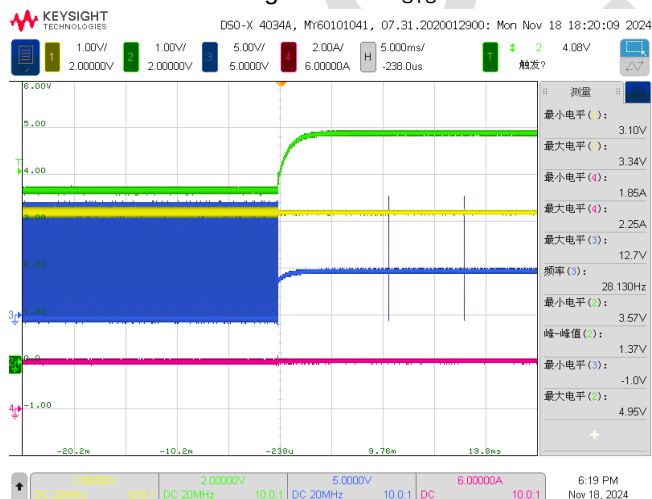
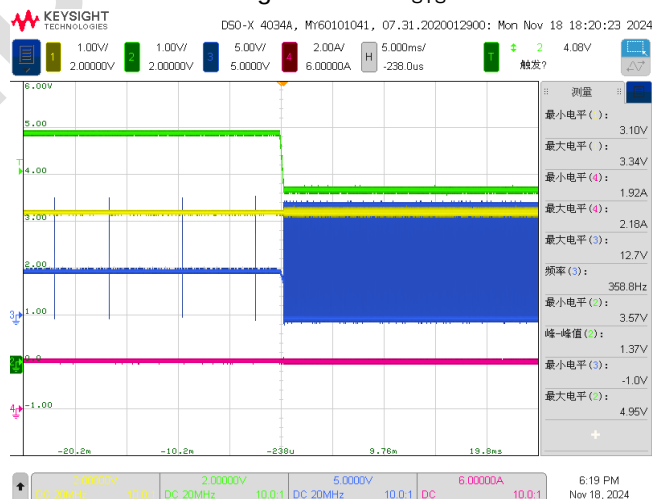
2.21 VBUS OVP

Test conditions: OVP set to 14V, $V_{BUS}=5V$, $V_{BAT}=3.8V$, $I_{CHG_SET}=2040mA$, charge enable, V_{BUS} ramp to 14.5V.

V_{BUS}=5V to 14.5VCH1-V_{BUS}, CH2-V_{BAT}, CH3-V_{SW}, CH4-I_{CHG}V_{BUS}=14.5V to 5VCH1-V_{BUS}, CH2-V_{BAT}, CH3-V_{SW}, CH4-I_{CHG}

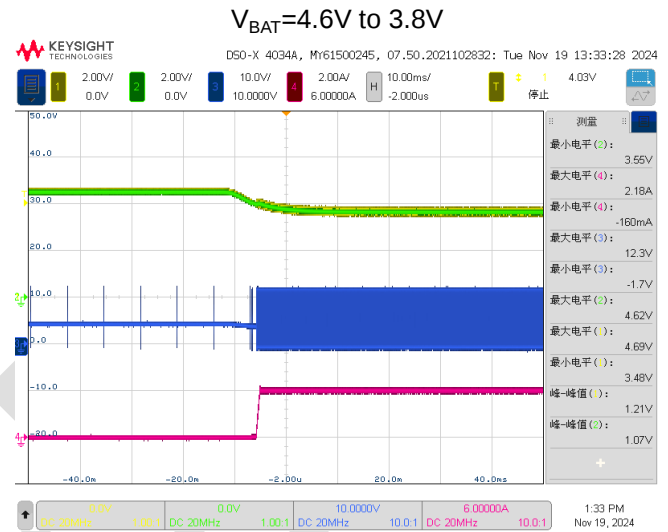
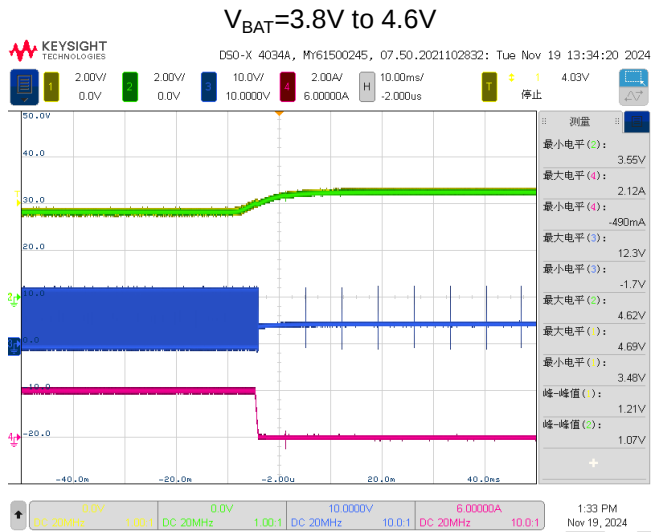
2.22 VSYS OVP

Test conditions: $V_{BUS}=12V$, $V_{BAT}=3.2V$, $I_{CHG_SET}=2040mA$, charge enable, $I_{SYS}=0A$, force a 5V external power supply on system.

Plug in 5V at V_{SYS}CH1-V_{BAT}, CH2-V_{SYS}, CH3-V_{SW}, CH4-I_{CHG}Plug out 5V at V_{SYS}CH1-V_{BAT}, CH2-V_{SYS}, CH3-V_{SW}, CH4-I_{CHG}

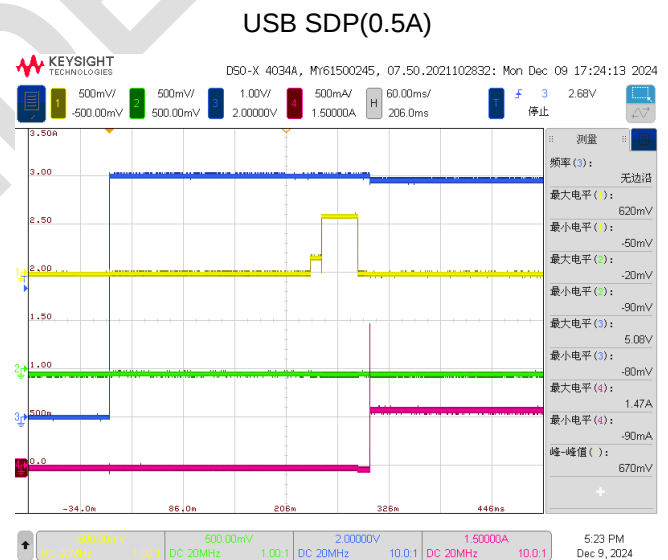
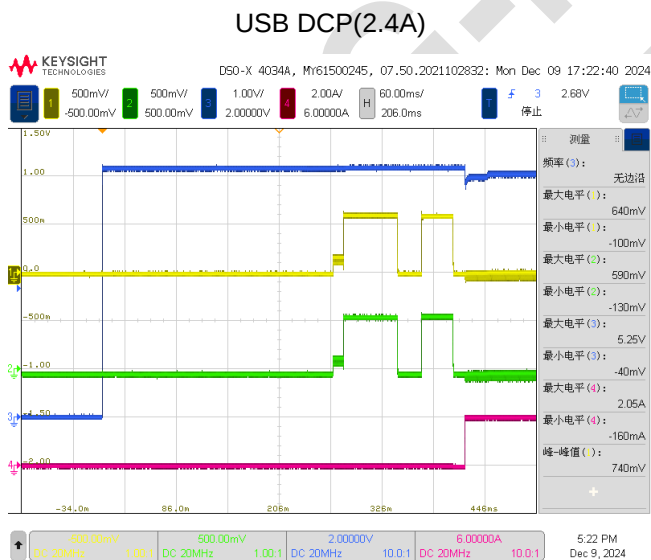
2.23 VBAT OVP

Test conditions: $V_{BUS}=12V$, $V_{BAT}=3.8V$, $I_{CHG_SET}=2040mA$, charge enable, $V_{REG}=4.2V$, V_{BAT} ramp to 4.6V.



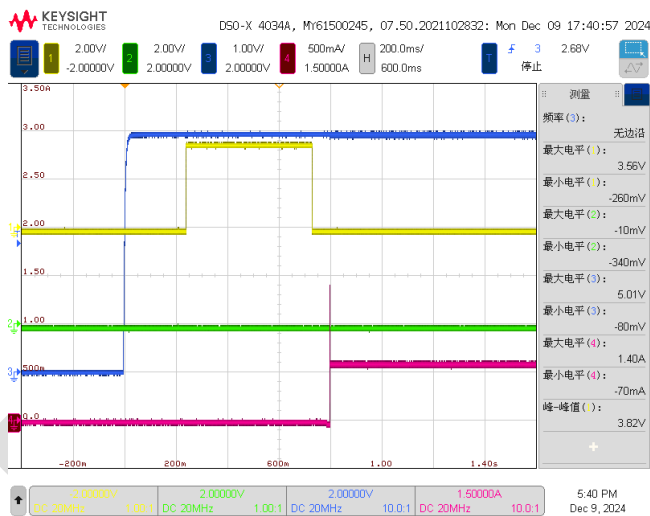
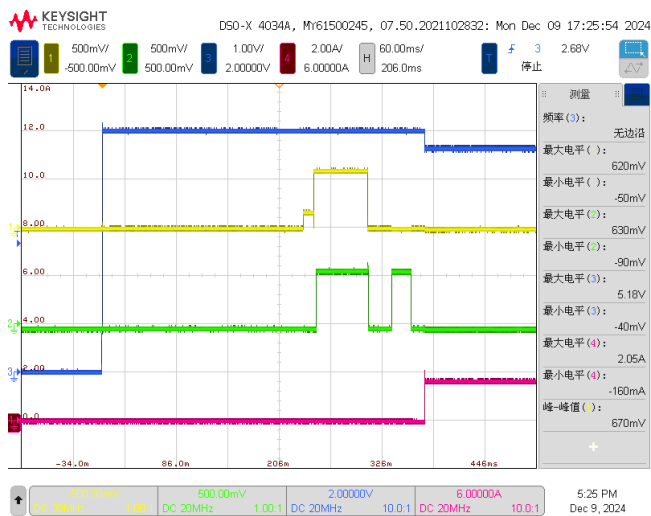
2.24 BC1.2 Detection

Test conditions: $V_{BAT}=3.8V$, $I_{CHG_SET}=2040mA$, charge enable, plug in different type adapter.



USB CDP(1.5A)

Unknown Adapter(0.5A)



CH1-D+, CH2-D-, CH3-V_{BUS}, CH4-I_{CHG}

CH1-D+, CH2-D-, CH3-V_{BUS}, CH4-I_{CHG}

2.25 Temperature Rise

Test conditions: V_{BAT}=3.8V, charge enable, measure the case temperature (T_c) rise with different input voltage and charge current.

